

**SMD464-4X16-11VS4 SDRAM SODIMM**

4MX64 SDRAM SO DIMM based on 4MX16, 4Banks, 4 Refresh, 3.3V DRAMs with SPD

**GENERAL DESCRIPTION**

The Advantage SMD464-4X16-11VS4 is a 4MX64 Synchronous Dynamic RAM high-density memory module. The Advantage SMD464-4X16-11VS4 consists of four CMOS 4MX16 bit with 4 Internal Banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF (or 0.22uF) decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The SMD464-4X16-11VS4 is a Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

**FEATURES**

- Performance range  
Max. Freq. (Speed): 66 MHz (10ns @ CL=3)
- Burst mode operation
- Auto and Self refresh capability
- LVTTTL compatible inputs and outputs
- Single 3.3V+/- 0.3V power supply
- MRS cycle with address key programs  
Latency (Access from column address)  
Burst length (1,2,4,8 & Full page)  
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB: **Height (1,150mil)**

**PIN CONFIGURATIONS (Front/Back)**

**PIN NAMES**

1	V <sub>SS</sub>	29	A0	57	NC	85	DQ17	113	V <sub>DD</sub>	141	**SDA
2	V <sub>SS</sub>	30	A3	58	NC	86	DQ49	114	V <sub>DD</sub>	142	**SCL
3	DQ0	31	A1	59	NC	87	DQ18	115	DQMB2	143	V <sub>DD</sub>
4	DQ32	32	A4	60	NC	88	DQ50	116	DQMB6	144	V <sub>DD</sub>
5	DQ1	33	A2	61	CLK0	89	DQ19	117	DQMB3		
6	DQ33	34	A5	62	CKE0	90	DQ51	118	DQMB7		
7	DQ2	35	V <sub>SS</sub>	63	V <sub>DD</sub>	91	V <sub>SS</sub>	119	V <sub>SS</sub>		
8	DQ34	36	V <sub>SS</sub>	64	V <sub>DD</sub>	92	V <sub>SS</sub>	120	V <sub>SS</sub>		
9	DQ3	37	DQ8	65	RAS	93	DQ20	121	DQ24		
10	DQ35	38	DQ40	66	CAS	94	DQ52	122	DQ56		
11	V <sub>DD</sub>	39	DQ9	67	WE	95	DQ21	123	DQ25		
12	V <sub>DD</sub>	40	DQ41	68	*CKE1	96	DQ53	124	DQ57		
13	DQ4	41	DQ10	69	CS0	97	DQ22	125	DQ26		
14	DQ36	42	DQ42	70	**A12	98	DQ54	126	DQ58		
15	DQ5	43	DQ11	71	*CS1	99	DQ23	127	DQ27		
16	DQ37	44	DQ43	72	*A13	100	DQ55	128	DQ59		
17	DQ6	45	V <sub>DD</sub>	73	DNU	101	V <sub>DD</sub>	129	V <sub>DD</sub>		
18	DQ38	46	V <sub>DD</sub>	74	CK1	102	V <sub>DD</sub>	130	V <sub>DD</sub>		
19	DQ7	47	DQ12	75	V <sub>SS</sub>	103	A6	131	DQ28		
20	DQ39	48	DQ44	76	V <sub>SS</sub>	104	A7	132	DQ60		
21	V <sub>SS</sub>	49	DQ13	77	NC	105	A8	133	DQ29		
22	V <sub>SS</sub>	50	DQ45	78	NC	106	BA0	134	DQ61		
23	DQMB0	51	DQ14	79	NC	107	V <sub>SS</sub>	135	DQ30		
24	DQMB4	52	DQ46	80	NC	108	V <sub>SS</sub>	136	DQ62		
25	DQMB1	53	DQ15	81	V <sub>DD</sub>	109	A9	137	DQ31		
26	DQMB5	54	DQ47	82	V <sub>DD</sub>	110	BA1	138	DQ63		
27	V <sub>DD</sub>	55	V <sub>SS</sub>	83	DQ16	111	A10	139	V <sub>SS</sub>		
28	V <sub>DD</sub>	56	V <sub>SS</sub>	84	DQ48	112	A11	140	V <sub>SS</sub>		

A0 ~ A11	Address input
BA0 ~ BA1	Select bank
DQ0~DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Col. address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
REF	Reserved for future
DU	Don't use

\*These pins are not used on this module  
 \*\*These pins should be NC in the system that does not support SPD



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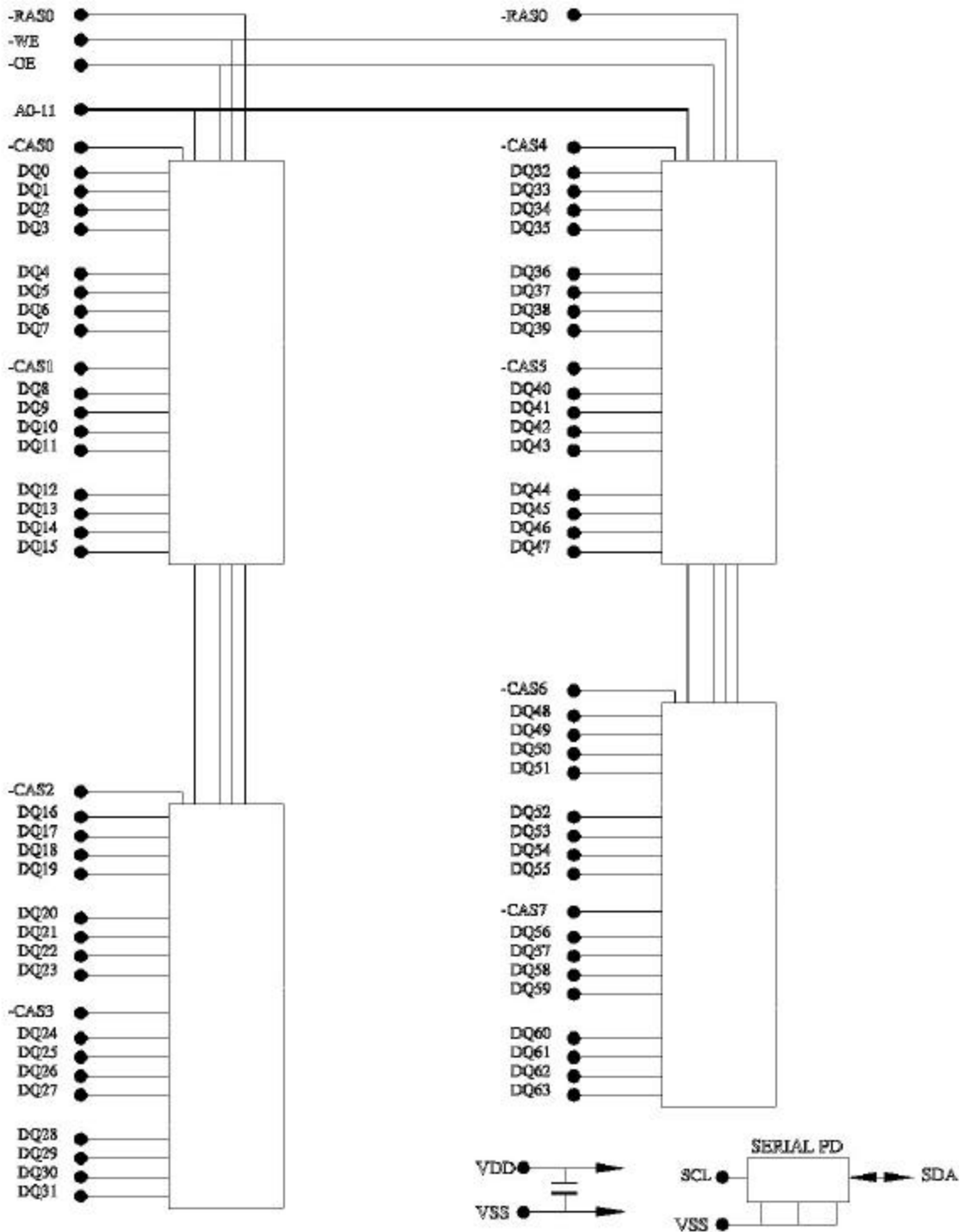
**PIN CONFIGURATION DESCRIPTION**

<b>Pin</b>	<b>Name</b>	<b>Input Function</b>
CLK	System clock	Active on the positive going edge to sample all inputs
CS	Chip select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0~A11	Address	Row/column addresses are multiplexed on the same pins. Row address: RA0~RA11, Column address: CA0~CA7.
BA0~BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
WE	Write enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0~7	Data input/output mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0~63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.



FUNCTIONAL BLOCK DIAGRAM

144 PIN, UNBUFFERED X64 DRAM DIMM, 1 BANK WITH X16 DRAMs



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## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V <sub>ss</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on V <sub>DD</sub> supply relative to V <sub>ss</sub>	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 4.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>d</sub>	4	W
Short circuit current	I <sub>OS</sub>	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V <sub>DD</sub> , V <sub>DDQ</sub>	3.0	3.3	3.6	V	
Input logic high voltage	V <sub>IH</sub>	2.0	3.0	V <sub>DDQ</sub> +0.3	V	1
Input logic low voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output logic high voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -2mA
Output logic low voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA
Input leakage (Inputs)	I <sub>IL</sub>	-10	-	10	uA	3
Input leakage (I/O pins)	I <sub>L</sub>	-10	-	10	uA	3,4

1. V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is  $\leq$  3ns.
2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is  $\leq$  3ns.
3. Any input 0V  $\leq$  V<sub>IN</sub>  $\leq$  V<sub>DDQ</sub>. Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. D<sub>out</sub> is disabled, 0V  $\leq$  V<sub>OUT</sub>  $\leq$  V<sub>DDQ</sub>.

## CAPACITANCE (V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 23°C, f = 1MHz, V<sub>REF</sub> = 1.4V $\pm$ 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A11, BA0 ~ BA1)	C <sub>ADD</sub>	15	25	pF
RAS, CAS, WE	C <sub>IN</sub>	15	25	pF
CKE (CKE0 ~ CKE1)	C <sub>CKE</sub>	15	25	pF
Clock (CLK0 ~ CLK3)	C <sub>CLK</sub>	10	13	pF
CS (CS0 ~ CS3)	C <sub>CS</sub>	10	15	pF
DQM (DQMB0 ~ DQMB7)	C <sub>DQM</sub>	8	10	pF
DQ (DQ0 ~ DQ63)	C <sub>OUT1</sub>	9	12	pF



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**DC CHARACTERISTICS**(Recommended operating condition unless otherwise noted,  $T_A = 0$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Test Condition	CAS Latency	Version -10	Unit	Note
Operating current	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\text{min})$ $I_{OL} = 0$ mA		400	mA	1
Precharge standby current	ICC2P	$\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 15\text{ns}$		4	mA	3
Precharge standby current	ICC2PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$		4	mA	3
Precharge standby current	ICC2N	$\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CS} \geq V_{IH}(\text{min})$ , $t_{CC} = 15\text{ns}$ Input signals are changed one time during 30ns		60	mA	4
Precharge standby current	ICC2NS	$\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$ Input signals are stable		24	mA	4
Active standby current	ICC3P	$\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CC} = 15\text{ns}$		12	mA	3
Active standby current	ICC3PS	$\text{CKE} \ \& \ \text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$		12	mA	3
Active standby current	ICC3N	$\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CS} \geq V_{IH}(\text{min})$ , $t_{CC} = 15\text{ns}$ Input signals are changed one time during 30ns		100	mA	4,5
Active standby current	ICC3NS	$\text{CKE} \geq V_{IH}(\text{min})$ , $\text{CLK} \leq V_{IL}(\text{max})$ , $t_{CC} = \infty$ Input signals are stable		60	mA	4,5
Operating Current	ICC4	$I_{OL} = 0$ mA Page burst 2Banks activated $t_{CCD} = 2\text{CLKs}$	CL=3	440	mA	1,6
			CL=2	440	mA	1,6
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\text{min})$		500	mA	2
Self refresh current	ICC6	$\text{CKE} \leq 0.2\text{V}$		4	mA	

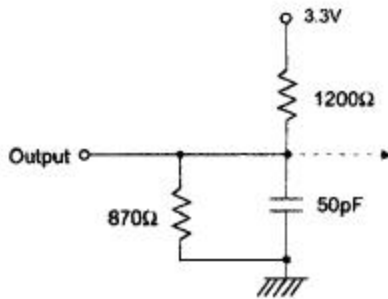
1. Measured with outputs open
2. Refresh period 64ms
3. Power-power mode
4. Non-power-down mode
5. One bank active
6. Burst mode



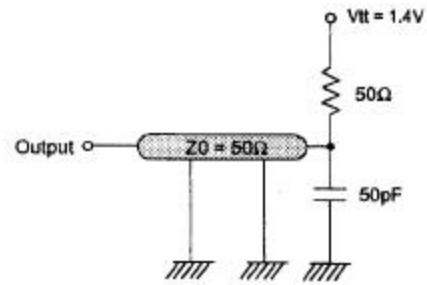
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**AC OPERATING TEST CONDITIONS** ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0$  to  $70^{\circ}C$ )

Parameter	Value	Unit
AC input levels ( $V_{ih}/V_{il}$ )	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

**OPERATING AC PARAMETER**

Parameter	Symbol	Version -10	Unit	Note
Row active to row active delay	$t_{RRD}(\min)$	20	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	24	ns	1
Row precharge time	$t_{RP}(\min)$	24	ns	1
Row active time	$t_{RAS}(\min)$	50	ns	1
Row active time	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	80	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data CL=3		2	each	4
Number of valid output data CL=2		1	each	4

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.



## AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
CLK cycle time CL=3	tCC	10	1000	ns	1
CLK cycle time CL=2	tCC	10	1000	ns	1
CLK to valid output delay	tSAC		7	ns	4
CLK to valid output delay	tSAC		7	ns	5
Output data hold time	tOHE	3		ns	4
Output data hold time	tOHE	3		ns	5
CLK high pulse width	tCH	3.5		ns	3
CLK low pulse width	tCL	3.5		ns	3
Input setup time	tSS	2.5		ns	3
Input hold time	tSH	1.5		ns	3
CLK to output in Low-Z	tSLZ	1		ns	2
CLK to output to Hi-Z	tSHZ		7	ns	4
CLK to output to Hi-Z	tSHZ		7	ns	5

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns,  $(tr/2-0.5)$ ns should be added to the parameter.
3. Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns. If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered, i.e.,  $[(tr + tf)/2-1]$ ns should be added to the parameter.
4. CL=3
5. CL=2



TRUTH TABLE

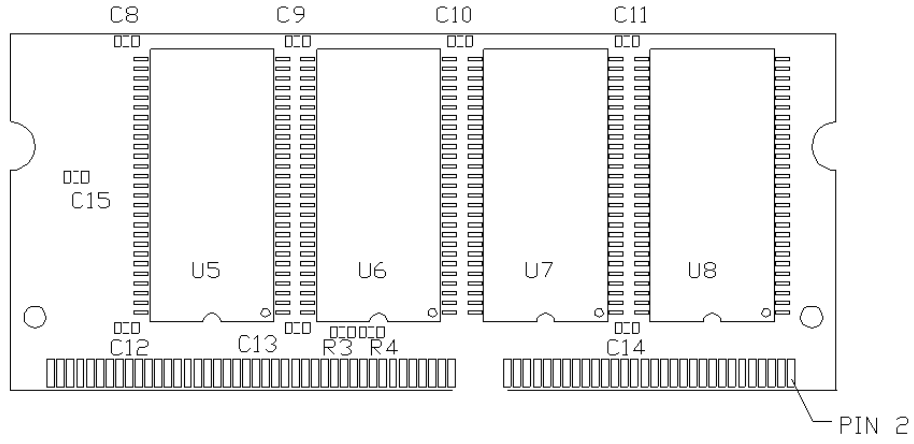
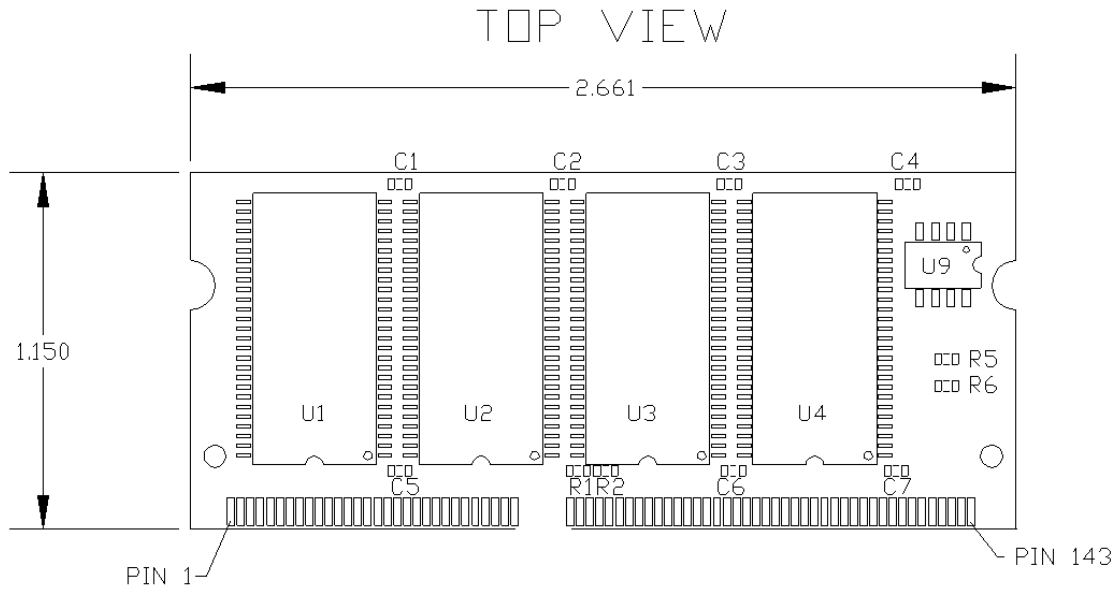
Command		CKEn-1	CKEn	CS	RAS	CAS	WE	DQM	BA0,1	A10/AP	A11,A9-A0	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3
	Self refresh	Entry	L	L	L	H	H	X	X			3
			Exit	L	H	L	H	H	H	X	X	
		H		X	X	X						
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A2-A9, A11)	4
	Auto precharge enable											H
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A2-A9, A11)	4
	Auto precharge enable											H
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks											X
Clock suspend or active power down	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
Precharge power down mode	Exit	L	H	X	X	X	X	X	X			
				L	H	H	H					
	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
Exit	L	H	H	X	X	X	X	X				
			L	V	V	V						
DQM		H	X					V	X			7
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

- OP Code : Operand code A<sub>0</sub> ~ A<sub>11</sub> & BA<sub>0</sub> ~ BA<sub>1</sub>: Program keys. (@ MRS)
- MRS can be issued only at all banks precharge state. A new command can be issued after 2 clock cycles of MRS.
- Auto refresh functions are as same as CBR refresh of DRAM.  
The automatical precharge without row precharge command is meant by "Auto". Auto/self refresh can be issued only at all banks precharge state.
- BA<sub>0</sub> ~ BA<sub>1</sub>: Bank select addresses.  
If both BA<sub>0</sub> and BA<sub>1</sub> are "Low" at read, write, row active and precharge, bank A is selected.  
If both BA<sub>0</sub> is "Low" and BA<sub>1</sub> is "High" at read, write, row active and precharge, bank B is selected.  
If both BA<sub>0</sub> is "High" and BA<sub>1</sub> is "Low" at read, write, row active and precharge, bank C is selected.  
If both BA<sub>0</sub> and BA<sub>1</sub> are "High" at read, write, row active and precharge, bank D is selected.  
If A<sub>10</sub>/AP is "High" at row precharge, BA<sub>0</sub> and BA<sub>1</sub> is ignored and all banks are selected.
- During burst read or write with auto precharge, new read/write command can not be issued. Another bank read/write command can be issued after the end of burst. New row active of the associated bank can be issued at t<sub>RP</sub> after the end of burst.
- Burst stop command is valid at every burst length.
- DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)



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BOTTOM VIEW



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