

EDC3272-16X4-66VNBS4 DRAM DIMM

32MX72 Unbuffered EDO DIMM with ECC based on 16MX4, 4K Refresh, 3.3V DRAMs

GENERAL DESCRIPTION

The Advantage EDC3272-16X4-66VNBS4 is a JEDEC standard 32MX72 bit Dynamic RAM high density memory module. The Advantage EDC3272-16X4-66VNBS4 consists of thirty-six CMOS 16MX4 TSOP-II 400mil, EDO Mode DRAM mounted on a 168-pin glass-epoxy substrate. One 0.1uF (or 0.22uF) decoupling capacitor is mounted on the printed circuit board in parallel for each DRAM. The EDC3272-16X4-66VNBS4 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

FEATURES

| | |
|------------------------------|--|
| Row Access Time | 60ns |
| Column Access Time | 17ns |
| Random Read/Write Cycle Time | 104ns |
| Page Mode Cycle Time | 25ns |
| Refresh Type | CAS before RAS (CBR), RAS only, Hidden Refresh |
| Refresh Rate | 4096 cycles in 64ms |
| Access Cycle | EDO PAGE MODE |
| Height | (1,950mil) |

PIN CONFIGURATIONS (FRONT/BACK)

PIN NAMES

| | | | | | | | | | | | | | |
|----|------|----|------|----|------|-----|------|-----|------|-----|------|-----------|-------------------------|
| 1 | VSS | 30 | RAS0 | 59 | VDD | 88 | DQ34 | 117 | A1 | 146 | RFU | A0-A11 | Address Input |
| 2 | DQ0 | 31 | OE0 | 60 | DQ20 | 89 | DQ35 | 118 | A3 | 147 | NC | DQ0-DQ63 | Data In/Out |
| 3 | DQ1 | 32 | VSS | 61 | NC | 90 | VDD | 119 | A5 | 148 | VSS | W0, W2 | Read/Write Enable |
| 4 | DQ2 | 33 | A0 | 62 | RFU | 91 | DQ36 | 120 | A7 | 149 | DQ53 | OE0, OE2 | Output Enable |
| 5 | DQ3 | 34 | A2 | 63 | NC | 92 | DQ37 | 121 | A9 | 150 | DQ54 | RAS0-RAS3 | Row Address Strobe |
| 6 | VDD | 35 | A4 | 64 | VSS | 93 | DQ38 | 122 | A11 | 151 | DQ55 | CAS0-CAS7 | Column Address Strobe |
| 7 | DQ4 | 36 | A6 | 65 | DQ21 | 94 | DQ39 | 123 | NC | 152 | VSS | VDD | Power (+3.3V) |
| 8 | DQ5 | 37 | A8 | 66 | DQ22 | 95 | DQ40 | 124 | VDD | 153 | DQ56 | VSS | Ground |
| 9 | DQ6 | 38 | A10 | 67 | DQ23 | 96 | VSS | 125 | RFU | 154 | DQ57 | NC | No Connection |
| 10 | DQ7 | 39 | NC | 68 | VSS | 97 | DQ41 | 126 | RFU | 155 | DQ58 | DU | Don't Use |
| 11 | DQ8 | 40 | VDD | 69 | DQ24 | 98 | DQ42 | 127 | VSS | 156 | DQ59 | SDA | Serial Address/Data I/O |
| 12 | VSS | 41 | VDD | 70 | DQ25 | 99 | DQ43 | 128 | RFU | 157 | VDD | SCL | Serial Clock |
| 13 | DQ9 | 42 | RFU | 71 | DQ26 | 100 | DQ44 | 129 | NC | 158 | DQ60 | SA0-SA2 | Address in EEPROM |
| 14 | DQ10 | 43 | VSS | 72 | DQ27 | 101 | DQ45 | 130 | CAS6 | 159 | DQ61 | CB0-CB7 | Check Bit |
| 15 | DQ11 | 44 | OE2 | 73 | VDD | 102 | VDD | 131 | CAS7 | 160 | DQ62 | | |
| 16 | DQ12 | 45 | RAS2 | 74 | DQ28 | 103 | DQ46 | 132 | RFU | 161 | DQ63 | | |
| 17 | DQ13 | 46 | CAS2 | 75 | DQ29 | 104 | DQ47 | 133 | VDD | 162 | VSS | | |
| 18 | VDD | 47 | CAS3 | 76 | DQ30 | 105 | CB4 | 134 | NC | 163 | NC | | |
| 19 | DQ14 | 48 | WE2 | 77 | DQ31 | 106 | CB5 | 135 | NC | 164 | NC | | |
| 20 | DQ15 | 49 | VDD | 78 | VSS | 107 | VSS | 136 | CB6 | 165 | SA0 | | |
| 21 | CB0 | 50 | NC | 79 | NC | 108 | NC | 137 | CB7 | 166 | SA1 | | |
| 22 | CB1 | 51 | NC | 80 | NC | 109 | NC | 138 | VSS | 167 | SA2 | | |
| 23 | VSS | 52 | CB2 | 81 | NC | 110 | VDD | 139 | DQ48 | 168 | VDD | | |
| 24 | NC | 53 | CB3 | 82 | SDA | 111 | RFU | 140 | DQ49 | | | | |
| 25 | NC | 54 | VSS | 83 | SCL | 112 | CAS4 | 141 | DQ50 | | | | |
| 26 | VDD | 55 | DQ16 | 84 | VDD | 113 | CAS5 | 142 | DQ51 | | | | |
| 27 | WE0 | 56 | DQ17 | 85 | VSS | 114 | NC | 143 | VDD | | | | |
| 28 | CAS0 | 57 | DQ18 | 86 | DQ32 | 115 | RFU | 144 | DQ52 | | | | |
| 29 | CAS1 | 58 | DQ19 | 87 | DQ33 | 116 | VSS | 145 | NC | | | | |



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PIN DESCRIPTIONS

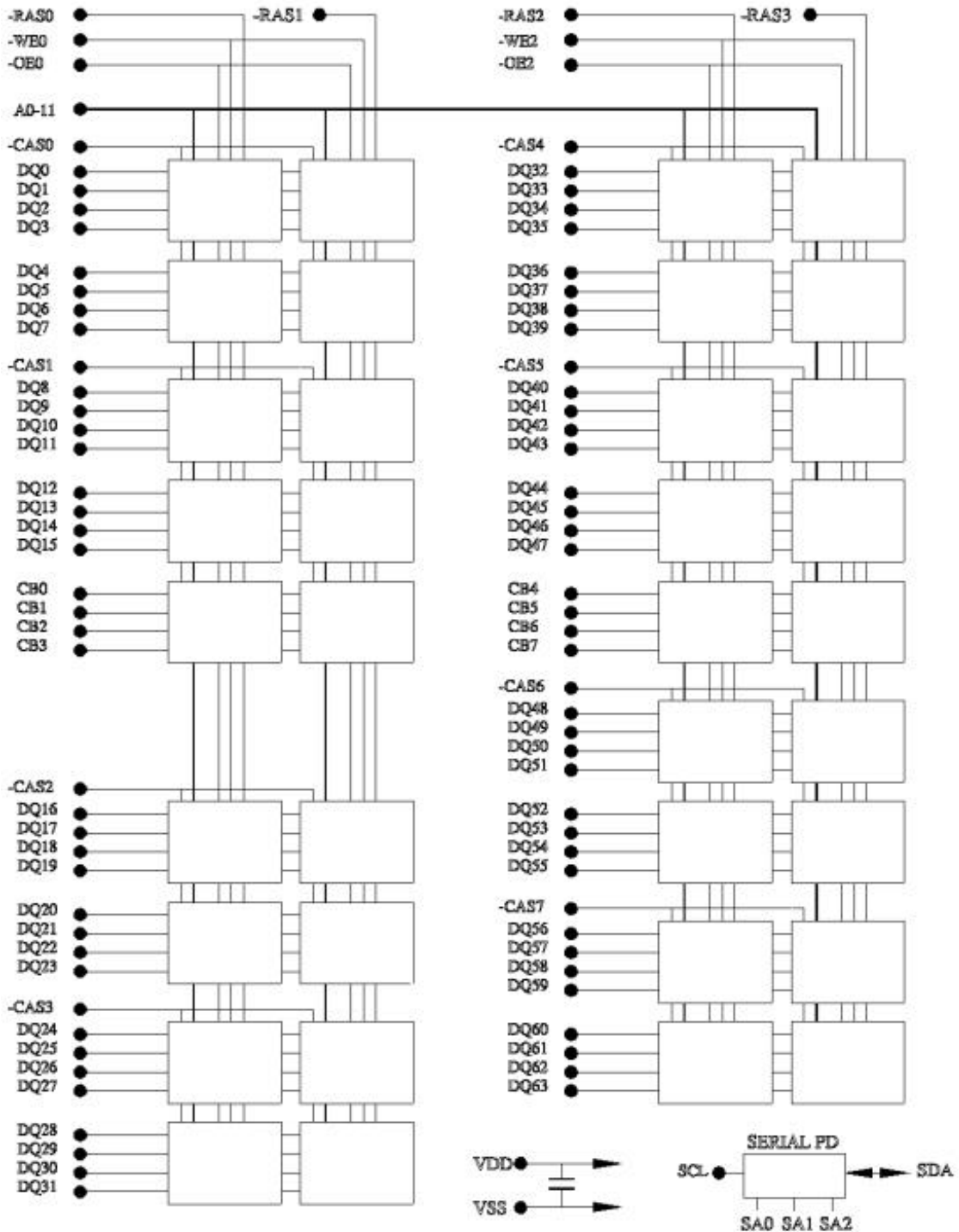
| PIN NUMBERS | SYMBOL | TYPE | DESCRIPTION |
|---|-----------------|--------------|---|
| 30, 45, 114, 129 | RAS0-RAS3 | Input | Row-Address Strobe: RAS is used to clock-in the row address bits. Two RAS inputs allow for one x72 bank or two x36 banks. |
| 28, 29, 46, 47, 112, 113, 130, 131 | CAS0-CAS7 | Input | Column-Address Strobe: CAS is used to clock-in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight CAS inputs allow byte access control for any memory bank configuration. |
| 27, 48 | WE0, WE2 | Input | Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle. |
| 31,44 | OE0-OE2 | Input | Output Enable: OE is the input/output control for the DQ pins. These signals may be driven, allowing LATE WRITE cycles. |
| 33-38, 117-122 | A0-A11 | Input | Address Inputs: These inputs are multiplexed and clocked by RAS and CAS. |
| 2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161 | DQ0-DQ63 | Input/Output | Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location. |
| 21-22, 52-53, 105-106, 136-137 | CB0-CB7 | Input/Output | Check Bits. |
| 42, 62, 111, 115, 125-126, 128, 132, 146 | RFU | - | Reserved for Future Use: These pins should be left unconnected. |
| 6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168 | V _{DD} | Supply | Power Supply: +3.3V ±0.3V |
| 1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162 | V _{SS} | Supply | Ground |
| 82 | SDA | Input/Output | Serial Presence-Detect Data. SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module. |
| 83 | SCL | Input | Serial Clock for Presence-Detect. SCL is used to synchronize the presence-detect data transfer to and from the module. |
| 165-167 | SA0-SA2 | Input | Presence-Detect Address Inputs. These pins are used to configure the presence-detect device. |



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BLOCK DIAGRAM

168 PIN, UNBUFFERED X72 ECC DRAM DIMM, 2 BANK WITH X4 DRAMs



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ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|---------------------------------------|------------------------------------|------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -1.0 ~ 4.6 | |
| Voltage on VDD supply relative to Vss | V _{DD} , V _{DDQ} | -1.0 ~ 4.6 | |
| Storage temperature | T _{STG} | -55 ~ +125 | |
| Short circuit current | I _{OS} | 50 | |

DC OPERATING CONDITIONS

(V_{DD} = +3.3V ±0.3V)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS |
|------------------------|--------|------|----------|-------|
| SUPPLY VOLTAGE | VCC | 3 | 3.6 | V |
| INPUT HIGH VOLTAGE | VIH | 2 | VDD +0.3 | V |
| INPUT LOW VOLTAGE | VIL | -0.5 | 0.8 | V |
| INPUT LEAKAGE CURRENT | I(IL) | -18 | 18 | Ua |
| OUTPUT LEAKAGE CURRENT | I(OL) | -5 | 5 | Ua |

DC OPERATING CHARACTERISTICS

(V_{DD} = +3.3V ±0.3V)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS |
|---|--------|-----|-------|-------|
| OPERATING CURRENT (RAS, CAS, Address cycling @tRC=min) | ICC1 | - | 1,998 | mA |
| STANDBY CURRENT (RAS=CAS=VIH) | ICC2 | - | 36 | mA |
| RAS ONLY REFRESH CURRENT (CAS=VIH, RAS cycling @ tRC=min) | ICC3 | - | 1,988 | mA |
| EDO PAGE MODE CURRENT (RAS=VIL, CAS cycling: tHPC=min) | ICC4 | - | 1,638 | mA |
| STANDBY CURRENT (RAS=CAS=VCC-0.2V) | ICC5 | - | 18 | mA |
| CAS BEFORE RAS REFRESH CURRENT (RAS and CAS cycling @tRC=min) | ICC6 | - | 1,988 | mA |
| OUTPUT HIGH VOLTAGE LEVEL (I _{OH} = -2mA) | VOH | 2.4 | - | V |
| OUTPUT LOW VOLTAGE LEVEL (I _{OL} = 2mA) | VOL | | 0.4 | V |

CAPACITANCE

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|--|--------|-----|-----|------|
| Input Capacitance [A0-A11] | CIN1 | - | 190 | pF |
| Input Capacitance [WE0, WE2, OE0, OE2] | CIN2 | - | 136 | pF |
| Input Capacitance [RAS0-RAS3] | CIN3 | - | 73 | pF |
| Input Capacitance [CAS0-CAS7] | CIN4 | - | 52 | pF |
| Input/Output capacitance [DQ0-DQ63, SDA] | CDQ | - | 27 | pF |



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AC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|--------|-----|---------|------|
| Access time from column address | tAA | | 25 | ns |
| Column-address setup to CAS precharge during writes | tACH | 15 | | ns |
| Column-address hold time (referenced to RAS) | tAR | 45 | | ns |
| Column-address setup time | tASC | 0 | | ns |
| Row-address setup time | tASR | 0 | | ns |
| Column address to WE delay time | tAWD | 45 | | ns |
| Access time from CAS | tCAC | | 13 | ns |
| Column-address hold time | tCAH | 7 | | ns |
| CAS pulse width | tCAS | 8 | 10,000 | ns |
| CAS hold time (CBR Refresh) | tCHR | 10 | | ns |
| CAS to output in Low-Z | tCLZ | 0 | | ns |
| Data output hold after CAS LOW | tCOH | 3 | | ns |
| CAS precharge time | tCP | 7 | | ns |
| Access time from CAS precharge | tCPA | | 28 | ns |
| CAS to RAS precharge time | tCRP | 5 | | ns |
| CAS hold time | tCSH | 38 | | ns |
| CAS setup time (CBR Refresh) | tCSR | 5 | | ns |
| CAS to WE delay time | tCWD | 33 | | ns |
| WRITE command to CAS lead time | tCWL | 7 | | ns |
| Data-in hold time | tDH | 7 | | ns |
| Data-in setup time | tDS | 0 | | ns |
| Output disable | tOD | 0 | 15 | ns |
| Output enable | tOE | | 15 | ns |
| OE hold time from WE during READ-MODIFY-WRITE cycle | tOEH | 10 | | ns |
| OE HIGH hold time from CAS HIGH | tOEHC | 10 | | ns |
| OE HIGH pulse width | tOEP | 5 | | ns |
| OE LOW to CAS HIGH setup time | tOES | 5 | | ns |
| Output buffer turn-off delay | tOFF | 0 | 15 | ns |
| OE setup prior to RAS during HIDDEN REFRESH cycle | tORD | 0 | | ns |
| EDO-PAGE-MODE READ or WRITE cycle time | tPC | 20 | | ns |
| EDO-PAGE-MODE READ-WRITE cycle time | tPRWC | 67 | | ns |
| Access time from RAS | tRAC | | 50 | ns |
| RAS to column-address delay time | tRAD | 12 | 25 | ns |
| Row-address hold time | tRAH | 10 | | ns |
| RAS pulse width (EDO PAGE MODE) | tRASP | 50 | 200,000 | ns |
| Random READ or WRITE cycle time | tRC | 84 | | ns |
| RAS to CAS delay time | tRCD | 17 | 37 | ns |
| READ command hold time (referenced to CAS) | tRCH | 0 | | ns |
| READ command setup time | tRCS | 0 | | ns |
| Refresh period (4,096 cycles) | tREF | | 64 | ms |



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AC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|--------|-----|-----|------|
| RAS precharge time | tRP | 30 | | ns |
| RAS to CAS precharge time | tRPC | 5 | | ns |
| READ command hold time (referenced to RAS) | tRRH | 0 | | ns |
| RAS hold time | tRSH | 8 | | ns |
| READ-WRITE cycle time | tRWC | 128 | | ns |
| RAS to WE delay time | tRWD | 84 | | ns |
| WRITE command to RAS lead time | tRWL | 15 | | ns |
| Transition time (rise or fall) | tT | 1 | 50 | ns |
| WRITE command hold time | tWCH | 10 | | ns |
| WRITE command hold time (referenced to RAS) | tWCR | 45 | | ns |
| WE command setup time | tWCS | 0 | | ns |
| Output disable delay from WE (CAS HIGH) | tWHZ | | 15 | ns |
| WRITE comand pulse width | tWP | 7 | | ns |
| WE pulse width for output disable when CAS HIGH | tWRH | 10 | | ns |
| WE holt time (CBR Refresh) | tWRP | 10 | | ns |
| WE pulse width for output disable when CAS HIGH | tWPZ | 10 | | ns |



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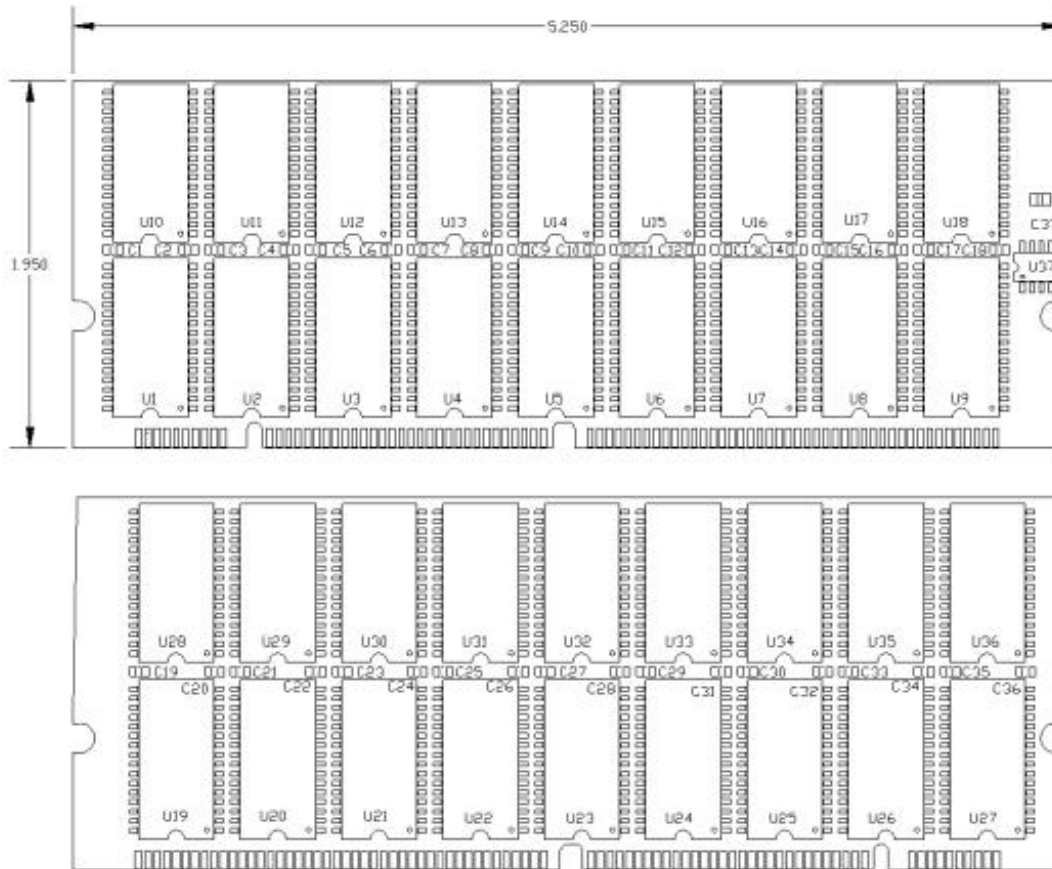
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. VDD = +3.3V; f = 1 MHz.
3. Ice is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100 μ s is required after power-up, followed by eight RAS# REFRESH cycles (RAS*-ONLY or CBR with WE* HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
7. AC characteristics assume tT = 2ns.
8. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
9. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
10. If CAS# and RAS# = VIH, data output is High-Z.
11. If CAS# = VIL, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and IOOpF and VOL = 0.8V and VOH = 2V.
13. Requires that *tAA and tCAC are not violated.
14. Requires that tAA and tRAC are not violated.
15. If CAS* is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ICP.
16. The tRCD (MAX) limit is no longer specified. tRCD (MAX) was specified as a reference point only. If tRCD was greater than the specified tRCD (MAX) limit, then access time was controlled exclusively by tCAC (tRAC [MIN] no longer applied). With or without the tRCD (MAX) limit, tAA and tCAC must always be met.
17. The tRAD (MAX) limit is no longer specified. tRAD (MAX) was specified as a reference point only. If tRAD was greater than the specified tRAD (MAX) limit, then access time was controlled exclusively by tAA (tRAC and tCAC no longer applied). With or without the tRAD (MAX) limit, tAA, tRAC and tCAC must always be met.
18. Either tRCH or tRRH must be satisfied for a READ cycle.
19. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE* = LOW and OE# = HIGH.
21. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
22. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. tWCS, tRWD, tAWD and tCWD are not restrictive operating parameters. *WCS applies to EARLY WRITE cycles. If WCS > tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. tRWD, tAWD and tCWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE# held HIGH and WE# taken LOW after CAS* goes LOW result in a LATE WRITE (OE#-controlled) cycle. tWCS, tRWD, tCWD and tAWD are not applicable in a LATE WRITE Cycle.
24. Column address changed once each cycle.
25. The 3ns minimum parameter guaranteed by design.
26. Measured with the specified current load and IOOpF.
27. tOFF on an EDO module is determined by the latter of the RAS# and CAS* signals to transition HIGH.
28. The SPD EEPROM WRITE cycle time (CWR) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit are disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
29. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
30. All other inputs at 0.2V or VDD - 0.2V.
31. VIH overshoot: VIH (MAX) = VDD + 2V for a pulse width < 10ns, and the pulse width cannot be greater than one third of the cycle rate. VIL undershoot: VIL (MIN) = -2V for a pulse width < 10ns, and the pulse width cannot be greater than one third of the cycle rate.



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ENGINEERING DRAWING



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