

## EDC3272-16X4-66VB8 DRAM DIMM

32MX72 Buffered EDO DIMM based on 16MX4, 8K Refresh, 3.3V DRAMs

### GENERAL DESCRIPTION

The Advantage EDC3272-16X4-66VB8 is a JEDEC standard 32MX72 bit Dynamic RAM high density memory module. The Advantage EDC3272-16X4-66VB8 consists of thirty-six CMOS 16MX4 TSOP-II 400mil, EDO Mode DRAM mounted on a 168-pin glass-epoxy substrate. Two 0.1uF (or 0.22uF) decoupling capacitors are mounted on the printed circuit board in parallel for each DRAM. The EDC3272-16X4-66VB8 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

### FEATURES

Row Access Time	60ns
Column Access Time	17ns
Random Read/Write Cycle Time	104ns
Page Mode Cycle Time	25ns
Refresh Type	CAS before RAS (CBR), RAS only, Hidden Refresh
Refresh Rate	8192 cycles in 64ms
Access Cycle	EDO PAGE MODE
Height	(2,000MIL)

### PIN CONFIGURATIONS (FRONT/BACK)

### PIN NAMES

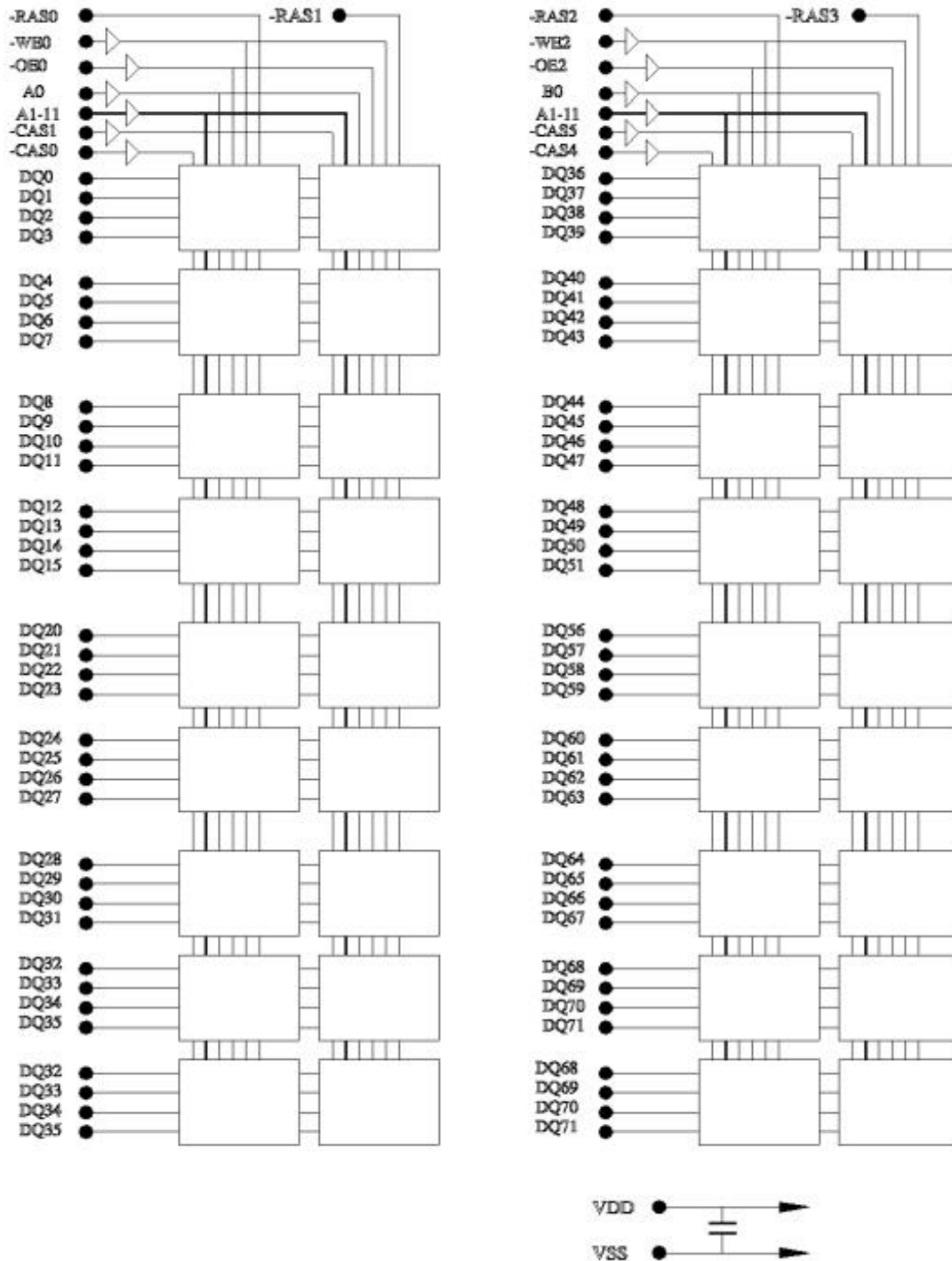
1	VSS	30	RAS0	59	VDD	88	DQ38	117	A1	146	RFU	A0-A11	Address Input
2	DQ0	31	OE0	60	DQ24	89	DQ39	118	A3	147	RFU	DQ0-DQ71	Data In/Out
3	DQ1	32	VSS	61	RFU	90	VDD	119	A5	148	RFU	W0, W2	Read/Write Enable
4	DQ2	33	A0	62	RFU	91	DQ40	120	A7	149	DQ61	OE0, OE2	Output Enable
5	DQ3	34	A2	63	RFU	92	DQ41	121	A9	150	DQ62	RAS0-RAS3	Row Address Strobe
6	VDD	35	A4	64	RFU	93	DQ42	122	A11	151	DQ63	CAS0, 1,4,5	Column Address Strobe
7	DQ4	36	A6	65	DQ25	94	DQ43	123	*A13	152	VSS	VDD	Power (+3.3V)
8	DQ5	37	A8	66	DQ26	95	DQ44	124	VDD	153	DQ64	VSS	Ground
9	DQ6	38	A10	67	DQ27	96	VSS	125	RFU	154	DQ65	NC	No Connection
10	DQ7	39	A12	68	VSS	97	DQ45	126	B0	155	DQ66	DU	Don't Use
11	DQ8	40	VDD	69	DQ28	98	DQ46	127	VSS	156	DQ67	PDE	Presence Detect Enable
12	VSS	41	RFU	70	DQ29	99	DQ47	128	RFU	157	VDD	PD1-8	Presence Detect
13	DQ9	42	RFU	71	DQ30	100	DQ48	129	RAS3	158	DQ68	RFU	Reserved for future use
14	DQ10	43	VSS	72	DQ31	101	DQ49	130	CAS5	159	DQ69	ID0-ID1	ID bit
15	DQ11	44	OE2	73	VDD	102	VDD	131	*CAS7	160	DQ70		
16	DQ12	45	RAS2	74	DQ32	103	DQ50	132	PDE	161	DQ71		
17	DQ13	46	CAS4	75	DQ33	104	DQ51	133	VDD	162	VSS		
18	VDD	47	*CAS6	76	DQ34	105	DQ52	134	NC	163	PD2		
19	DQ14	48	W2	77	DQ35	106	DQ53	135	NC	164	PD4		
20	DQ15	49	VDD	78	VSS	107	VSS	136	DQ54	165	PD6		
21	DQ16	50	NC	79	PD1	108	NC	137	DQ55	166	PD8		
22	DQ17	51	NC	80	PD3	109	NC	138	VSS	167	ID1		
23	VSS	52	DQ18	81	PD5	110	VDD	139	DQ56	168	VDD		
24	NC	53	DQ19	82	PD7	111	RFU	140	DQ57				
25	NC	54	VSS	83	ID0	112	CAS1	141	DQ58				
26	VDD	55	DQ20	84	VDD	113	CAS3	142	DQ59				
27	W0	56	DQ21	85	VSS	114	RAS1	143	VDD				
28	CAS0	57	DQ22	86	DQ36	115	RFU	144	DQ60				
29	*CAS2	58	DQ23	87	DQ37	116	VSS	145	RFU				



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BLOCK DIAGRAM

168 PIN, X72 BCC DRAM DIMM, 2 BANKS WITH X4 DRAMs



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**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	
Voltage on VDD supply relative to Vss	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 4.6	
Storage temperature	T <sub>STG</sub>	-55 ~ +125	
Short circuit current	I <sub>OS</sub>	50	

**DC OPERATING CONDITIONS**

(V<sub>DD</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	VCC	3	3.6	V
INPUT HIGH VOLTAGE	VIH	2	VDD +0.3	V
INPUT LOW VOLTAGE	VIL	-0.5	0.8	V
INPUT LEAKAGE CURRENT	I(IL)	-18	18	Ua
OUTPUT LEAKAGE CURRENT	I(OL)	-10	10	Ua

**DC OPERATING CHARACTERISTICS**

(V<sub>DD</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
OPERATING CURRENT (RAS, CAS, Address cycling @tRC=min)	ICC1	-	2,955	mA
STANDBY CURRENT (RAS=CAS=VIH)	ICC2	-	99	mA
RAS ONLY REFRESH CURRENT (CAS=VIH, RAS cycling @ tRC=min)	ICC3	-	2,955	mA
EDO PAGE MODE CURRENT (RAS=VIL, CAS cycling: tHPC=min)	ICC4	-	2,235	mA
STANDBY CURRENT (RAS=CAS=VCC-0.2V)	ICC5	-	18	mA
CAS BEFORE RAS REFRESH CURRENT (RAS and CAS cycling @tRC=min)	ICC6	-	2,955	mA
OUTPUT HIGH VOLTAGE LEVEL (I <sub>OH</sub> = -2mA)	VOH	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL (I <sub>OL</sub> = 2mA)	VOL		0.4	V

**CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Capacitance [A0-A11]	CIN1	-	9	pF
Input Capacitance [WE0, WE2, OE0, OE2]	CIN2	-	9	pF
Input Capacitance [RAS0-RAS3]	CIN3	-	67	pF
Input Capacitance [CAS0-CAS7]	CIN4	-	32	pF
Input/Output capacitance [DQ0-DQ71, SDA]	CDQ	-	22	pF



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**AC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	MIN	MAX	UNIT
Access time from column address	tAA		35	ns
Column-address setup to CAS precharge during writes	tACH	15		ns
Column-address hold time (referenced to RAS)	tAR	43		ns
Column-address setup time	tASC	2		ns
Row-address setup time	tASR	5		ns
Column address to WE delay time	tAWD	51		ns
Access time from CAS	tCAC		20	ns
Column-address hold time	tCAH	15		ns
CAS pulse width	tCAS	10	10,000	ns
CAS hold time (CBR Refresh)	tCHR	8		ns
CAS to output in Low-Z	tCLZ	2		ns
Data output hold after CAS LOW	tCOH	3		ns
CAS precharge time	tCP	10		ns
Access time from CAS precharge	tCPA		40	ns
CAS to RAS precharge time	tCRP	10		ns
CAS hold time	tCSH	43		ns
CAS setup time (CBR Refresh)	tCSR	7		ns
CAS to WE delay time	tCWD	37		ns
WRITE command to CAS lead time	tCWL	10		ns
Data-in hold time	tDH	15		ns
Data-in setup time	tDS	-2		ns
Output disable	tOD	0	15	ns
Output enable	tOE		15	ns
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	8		ns
OE HIGH hold time from CAS HIGH	tOEHC	10		ns
OE HIGH pulse width	tOEP	5		ns
OE LOW to CAS HIGH setup time	tOES	5		ns
Output buffer turn-off delay	tOFF	2	20	ns
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		ns
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		ns
PDE to valid presence-detect data	tPD		10	ns
PDE inactive to presence-detects inactive	tPDOFF	2		ns
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	58		ns
Access time from RAS	tRAC		60	ns
RAS to column-address delay time	tRAD	10		ns
Row-address hold time	tRAH	8		ns
RAS pulse width	tRAS	60	10,000	
RAS pulse width (EDO PAGE MODE)	tRASP	60	125,000	ns
Random READ or WRITE cycle time	tRC	104		ns
RAS to CAS delay time	tRCD	12		ns
READ command hold time (referenced to CAS)	tRCH	0		ns
READ command setup time	tRCS	0		ns
Refresh period (4,096 cycles)	tREF		64	ms



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**AC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	MIN	MAX	UNIT
RAS precharge time	tRP	40		ns
RAS to CAS precharge time	tRPC	5		ns
READ command hold time (referenced to RAS)	tRRH	0		ns
RAS hold time	tRSH	20		ns
READ-WRITE cycle time	tRWC	145		ns
RAS to WE delay time	tRWD	81		ns
WRITE command to RAS lead time	tRWL	20		ns
Transition time (rise or fall)	tT	2	50	ns
WRITE command hold time	tWCH	15		ns
WRITE command hold time (referenced to RAS)	tWCR	43		ns
WE command setup time	tWCS	2		ns
Output disable delay from WE (CAS HIGH)	tWHZ		20	ns
WRITE comand pulse width	tWP	5		ns
WE pulse width for output disable when CAS HIGH	tWRH	10		ns
WE holt time (CBR Refresh)	tWRP	8		ns
WE pulse width for output disable when CAS HIGH	tWPZ	12		ns



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## NOTES

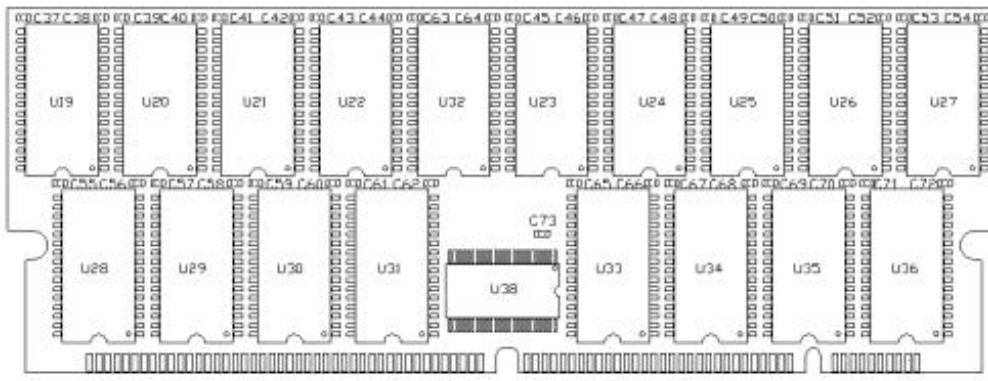
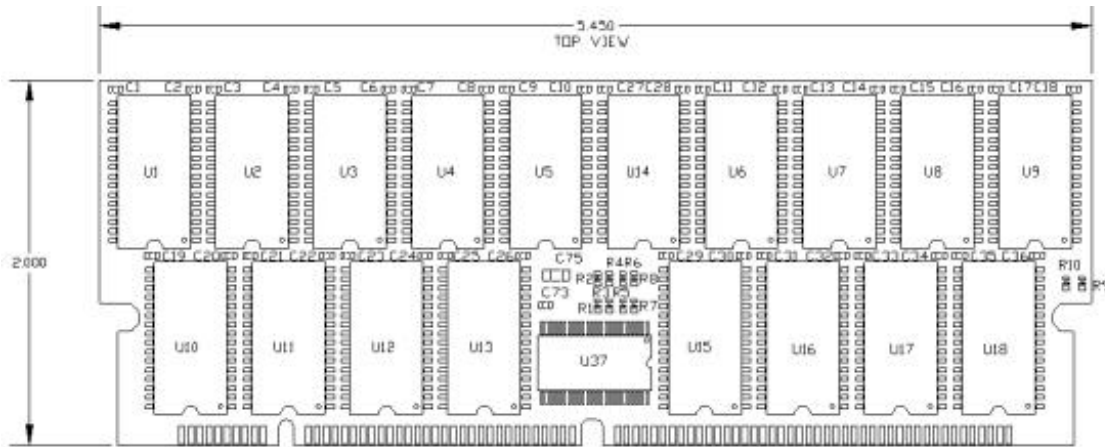
1. All voltages referenced to V<sub>SS</sub>.
2. This parameter is sampled. VDD = +3.3V; f = 1 MHz.
3. Ice is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100 $\mu$ s is required after power-up, followed by eight RAS# REFRESH cycles (RAS\*-ONLY or CBR with WE\* HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
7. AC characteristics assume t<sub>T</sub> = 2ns.
8. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
9. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
10. If CAS# and RAS# = VIH, data output is High-Z.
11. If CAS# = VIL, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and IO<sub>OP</sub>F and VOL = 0.8V and VOH = 2V.
13. Requires that \*-AA and 'CAC are not violated.
14. Requires that tAA and 'RAC are not violated.
15. If CAS\* is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ICP.
16. The tRCD (MAX) limit is no longer specified. tRCD (MAX) was specified as a reference point only. If tRCD was greater than the specified tRCD (MAX) limit, then access time was controlled exclusively by tCAC (tRAC [MIN] no longer applied). With or without the tRCD (MAX) limit, tAA and tCAC must always be met.
17. The tRAD (MAX) limit is no longer specified. tRAD (MAX) was specified as a reference point only. If tRAD was greater than the specified tRAD (MAX) limit, then access time was controlled exclusively by tAA (tRAC and \*CAC no longer applied). With or without the tRAD (MAX) limit, tAA, tRAC and 'CAC must always be met.
18. Either 'RCH or tRRH must be satisfied for a READ cycle.
19. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE\* = LOW and OE# = HIGH.
21. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
22. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. tWCS, tRWD, tAWD and 'CWD are not restrictive operating parameters. \*WCS applies to EARLY WRITE cycles. If WCS > tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. tRWD, tAWD and tCWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE# held HIGH and WE# taken LOW after CAS\* goes LOW result in a LATE WRITE (OE#-controlled) cycle. 'WCS, tRWD, tCWD and <AWD are not applicable in a LATE WRITE cycle.
24. Column address changed once each cycle.
25. The 3ns minimum parameter guaranteed by design.
26. Measured with the specified current load and IO<sub>OP</sub>F.
27. 'OFF on an EDO module is determined by the latter of the RAS# and CAS\* signals to transition HIGH.
28. The SPD EEPROM WRITE cycle time CWR) is the time from a valid stop condition of a write sequence to the end of the EEPROM Internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit are disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
29. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
30. All other inputs at 0.2V or VDD - 0.2V.
31. VIH overshoot: VIH (MAX) = VDD + 2V for a pulse width < 10ns, and the pulse width cannot be greater than one third of the cycle rate. VIL undershoot: VIL (MIN) = -2V for a pulse width < 10ns, and the pulse width cannot be greater than one third of the cycle rate.



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Revision: B 07/17/00

ENGINEERING DRAWING



BOTTOM VIEW



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