

ED3264-16X4-55VNBS4 DRAM DIMM

32MX64 Nonbuffered EDO DIMM based on 16MX4, 4K Refresh, 3.3V DRAMs

GENERAL DESCRIPTION

The Advantage ED3264-16X4-55VNBS4 is a JEDEC standard 16MX64 bit Dynamic RAM high density memory module. The Advantage ED3264-16X4-55VNBS4 consists of thirty-two CMOS 16MX4 TSOP-II 400mil, EDO Mode DRAM mounted on a 168-pin glass-epoxy substrate. Two 0.1uF (or 0.22uF) decoupling capacitors are mounted on the printed circuit board in parallel for each DRAM. The ED3264-16X4-55VNBS4 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

FEATURES

Row Access Time	50ns
Column Access Time	17ns
Random Read/Write Cycle Time	104ns
Page Mode Cycle Time	25ns
Refresh Type	CAS before RAS (CBR), RAS only, Hidden Refresh
Refresh Rate	4096 cycles in 64ms
Access Cycle	EDO PAGE MODE
Height	(1,950mil)

PIN CONFIGURATIONS (FRONT/BACK)

1	VSS	30	RAS0	59	VDD	88	DQ34	117	A1	146	RFU	
2	DQ0	31	OE0	60	DQ20	89	DQ35	118	A3	147	NC	
3	DQ1	32	VSS	61	NC	90	VDD	119	A5	148	VSS	
4	DQ2	33	A0	62	RFU	91	DQ36	120	A7	149	DQ53	
5	DQ3	34	A2	63	NC	92	DQ37	121	A9	150	DQ54	
6	VDD	35	A4	64	VSS	93	DQ38	122	A11	151	DQ55	
7	DQ4	36	A6	65	DQ21	94	DQ39	123	NC	152	VSS	
8	DQ5	37	A8	66	DQ22	95	DQ40	124	VDD	153	DQ56	
9	DQ6	38	A10	67	DQ23	96	VSS	125	RFU	154	DQ57	
10	DQ7	39	NC	68	VSS	97	DQ41	126	RFU	155	DQ58	
11	DQ8	40	VDD	69	DQ24	98	DQ42	127	VSS	156	DQ59	
12	VSS	41	VDD	70	DQ25	99	DQ43	128	RFU	157	VDD	
13	DQ9	42	RFU	71	DQ26	100	DQ44	129	NC	158	DQ60	
14	DQ10	43	VSS	72	DQ27	101	DQ45	130	CAS6	159	DQ61	
15	DQ11	44	OE2	73	VDD	102	VDD	131	CAS7	160	DQ62	
16	DQ12	45	RAS2	74	DQ28	103	DQ46	132	RFU	161	DQ63	
17	DQ13	46	CAS2	75	DQ29	104	DQ47	133	VDD	162	VSS	
18	VDD	47	CAS3	76	DQ30	105	*CB4	134	NC	163	NC	
19	DQ14	48	WE2	77	DQ31	106	*CB5	135	NC	164	NC	
20	DQ15	49	VDD	78	VSS	107	VSS	136	*CB6	165	SA0	
21	*CB0	50	NC	79	NC	108	NC	137	*CB7	166	SA1	
22	*CB1	51	NC	80	NC	109	NC	138	VSS	167	SA2	
23	VSS	52	*CB2	81	NC	110	VDD	139	DQ48	168	VDD	
24	NC	53	*CB3	82	SDA	111	RFU	140	DQ49			
25	NC	54	VSS	83	SCL	112	CAS4	141	DQ50			
26	VDD	55	DQ16	84	VDD	113	CAS5	142	DQ51			
27	WE0	56	DQ17	85	VSS	114	NC	143	VDD			
28	CAS0	57	DQ18	86	DQ32	115	RFU	144	DQ52			
29	CAS1	58	DQ19	87	DQ33	116	VSS	145	NC			

PIN NAMES

A0-A11	Address Input
DQ0-DQ63	Data In/Out
W0, W2	Read/Write Enable
OE0, OE2	Output Enable
RAS0-RAS3	Row Address Strobe
CAS0-CAS7	Column Address Strobe
VDD	Power (+3.3V)
VSS	Ground
NC	No Connection
DU	Don't Use
SDA	Serial Address/Data I/O
SCL	Serial Clock
SA0-SA2	Address in EEPROM

* These pins are not used in this module



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PIN DESCRIPTIONS

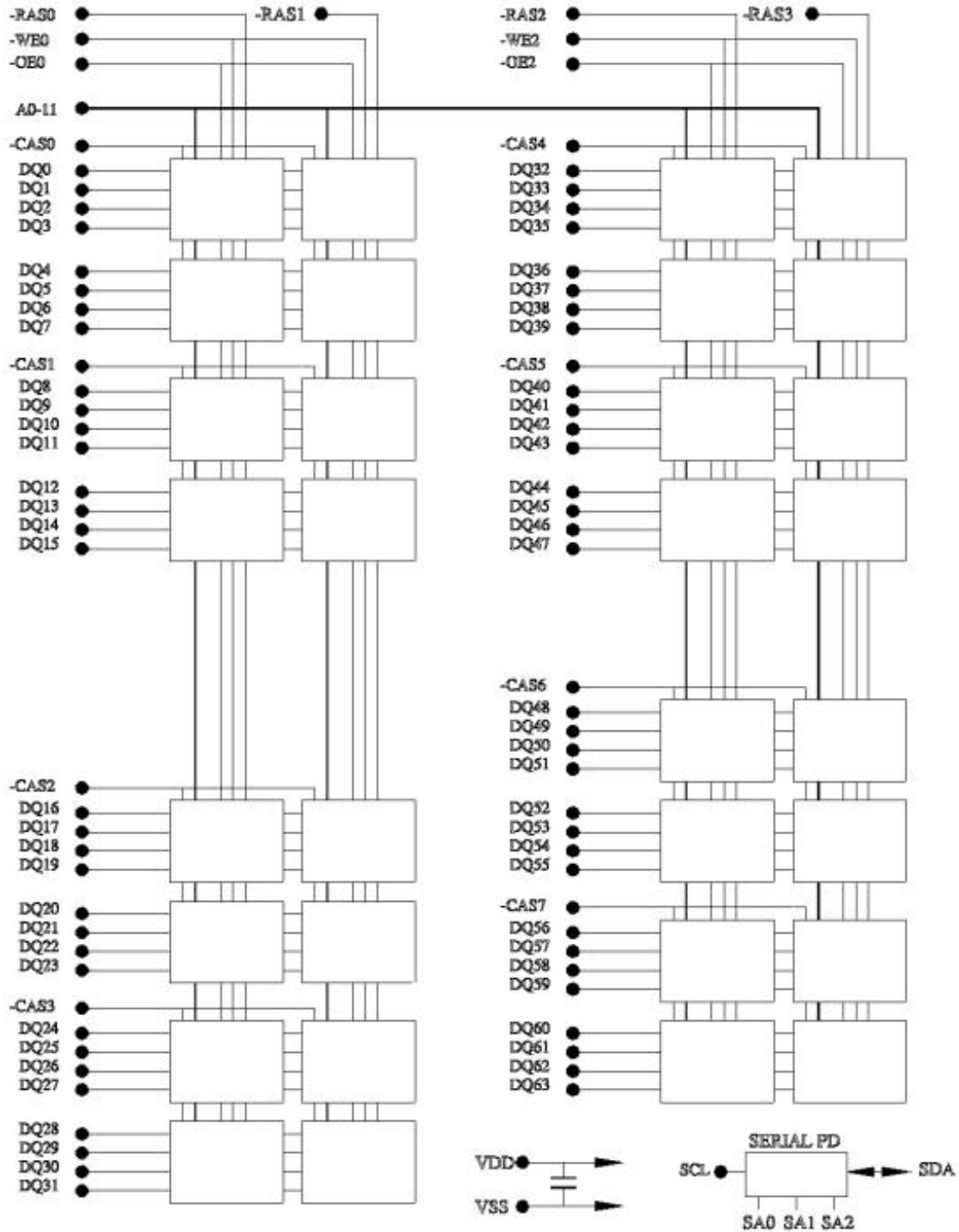
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45, 114, 129	RAS0-RAS3	Input	Row-Address Strobe: RAS is used to clock-in the row address bits. Two RAS inputs allow for one x72 bank or two x36 banks.
28, 29, 46, 47, 112, 113, 130, 131	CAS0-CAS7	Input	Column-Address Strobe: CAS is used to clock-in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight CAS inputs allow byte access control for any memory bank configuration.
27, 48	WE0, WE2	Input	Write Enable: WE is the READ/WRITE control for the DQ pins. If WE is LOW prior to CAS going LOW, the access is an EARLY WRITE cycle. If WE is HIGH while CAS is LOW, the access is a READ cycle, provided OE is also LOW. If WE goes LOW after CAS goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31,44	OE0-OE2	Input	Output Enable: OE is the input/output control for the DQ pins. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-122	A0-A11	Input	Address Inputs: These inputs are multiplexed and clocked by RAS and CAS.
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
21-22, 52-53, 105-106, 136-137	CB0-CB7	Input/Output	Check Bits.
42, 62, 111, 115, 125-126, 128, 132, 146	RFU	-	Reserved for Future Use: These pins should be left unconnected.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V _{DD}	Supply	Power Supply: +3.3V \pm 0.3V
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V _{SS}	Supply	Ground
82	SDA	Input/Output	Serial Presence-Detect Data. SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
83	SCL	Input	Serial Clock for Presence-Detect. SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs. These pins are used to configure the presence-detect device.



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BLOCK DIAGRAM

168 PIN, UNBUFFERED X64 DRAM DIMM, 2 BANK WITH X4 DRAMs



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	
Voltage on VDD supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 4.6	
Storage temperature	T _{STG}	-55 ~ +125	
Short circuit current	I _{OS}	50	

DC OPERATING CONDITIONS

(V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V _{CC}	3	3.6	V
INPUT HIGH VOLTAGE	V _{IH}	2	V _{DD} +0.3	V
INPUT LOW VOLTAGE	V _{IL}	-0.5	0.8	V
INPUT LEAKAGE CURRENT	I(I _L)	-18	18	Ua
OUTPUT LEAKAGE CURRENT	I(O _L)	-5	5	Ua

DC OPERATING CHARACTERISTICS

(V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
OPERATING CURRENT (RAS, CAS, Address cycling @t _{RC} =min)	ICC1	-	2,736	mA
STANDBY CURRENT (RAS=CAS=V _{IH})	ICC2	-	32	mA
RAS ONLY REFRESH CURRENT (CAS=V _{IH} , RAS cycling @ t _{RC} =min)	ICC3	-	2,736	mA
EDO PAGE MODE CURRENT (RAS=V _{IL} , CAS cycling: t _{HPC} =min)	ICC4	-	2,416	mA
STANDBY CURRENT (RAS=CAS=V _{CC} -0.2V)	ICC5	-	16	mA
CAS BEFORE RAS REFRESH CURRENT (RAS and CAS cycling @t _{RC} =min)	ICC6	-	2,736	mA
OUTPUT HIGH VOLTAGE LEVEL (I _{OH} = -2mA)	V _{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL (I _{OL} = 2mA)	V _{OL}		0.4	V

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Capacitance [A0-A11]	C _{IN1}	-	168	pF
Input Capacitance [WE0, WE2,OE0, OE2]	C _{IN2}	-	118	pF
Input Capacitance [RAS0-RAS3]	C _{IN3}	-	60	pF
Input Capacitance [CAS0-CAS7]	C _{IN4}	-	32	pF
Input Capacitance [SCL, SA0-SA2]	C _{IN5}	-	6	pF
Input/Output capacitance [DQ0-DQ63, SDA]	C _{DQ}	-	22	pF



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AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Access time from column address	tAA		25	ns
Column-address setup to CAS precharge during writes	tACH	12		ns
Column-address hold time (referenced to RAS)	tAR	38		ns
Column-address setup time	tASC	0		ns
Row-address setup time	tASR	0		ns
Column address to WE delay time	tAWD	42		ns
Access time from CAS	tCAC		13	ns
Column-address hold time	tCAH	8		ns
CAS pulse width	tCAS	8	10,000	ns
CAS hold time (CBR Refresh)	tCHR	8		ns
CAS to output in Low-Z	tCLZ	0		ns
Data output hold after CAS LOW	tCOH	3		ns
CAS precharge time	tCP	8		ns
Access time from CAS precharge	tCPA		28	ns
CAS to RAS precharge time	tCRP	5		ns
CAS hold time	tCSH	38		ns
CAS setup time (CBR Refresh)	tCSR	5		ns
CAS to WE delay time	tCWD	30		ns
WRITE command to CAS lead time	tCWL	8		ns
Data-in hold time	tDH	8		ns
Data-in setup time	tDS	0		ns
Output disable	tOD	0	12	ns
Output enable	tOE		12	ns
OE hold time from WE during READ-MODIFY-WRITE cycle	tOEH	8		ns
OE HIGH hold time from CAS HIGH	tOEHC	5		ns
OE HIGH pulse width	tOEP	5		ns
OE LOW to CAS HIGH setup time	tOES	4		ns
Output buffer turn-off delay	tOFF	0	12	ns
OE setup prior to RAS during HIDDEN REFRESH cycle	tORD	0		ns
EDO-PAGE-MODE READ or WRITE cycle time	tPC	20		ns
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	47		ns
Access time from RAS	tRAC		50	ns
RAS to column-address delay time	tRAD	9		ns
Row-address hold time	tRAH	9		ns
RAS pulse width (EDO PAGE MODE)	tRASP	50	125,000	ns
Random READ or WRITE cycle time	tRC	84		ns
RAS to CAS delay time	tRCD	11		ns
READ command hold time (referenced to CAS)	tRCH	0		ns
READ command setup time	tRCS	0		ns
Refresh period (4,096 cycles)	tREF		64	ms



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AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
RAS precharge time	tRP	30		ns
RAS to CAS precharge time	tRPC	5		ns
READ command hold time (referenced to RAS)	tRRH	0		ns
RAS hold time	tRSH	13		ns
READ-WRITE cycle time	tRWC	116		ns
RAS to WE delay time	tRWD	67		ns
WRITE command to RAS lead time	tRWL	13		ns
Transition time (rise or fall)	tT	2	50	ns
WRITE command hold time	tWCH	8		ns
WRITE command hold time (referenced to RAS)	tWCR	38		ns
WE command setup time	tWCS	0		ns
Output disable delay from WE (CAS HIGH)	tWHZ		12	ns
WRITE comand pulse width	tWP	5		ns
WE pulse width for output disable when CAS HIGH	tWRH	10		ns
WE holt time (CBR Refresh)	tWRP	8		ns
WE pulse width for output disable when CAS HIGH	tWPZ	8		ns



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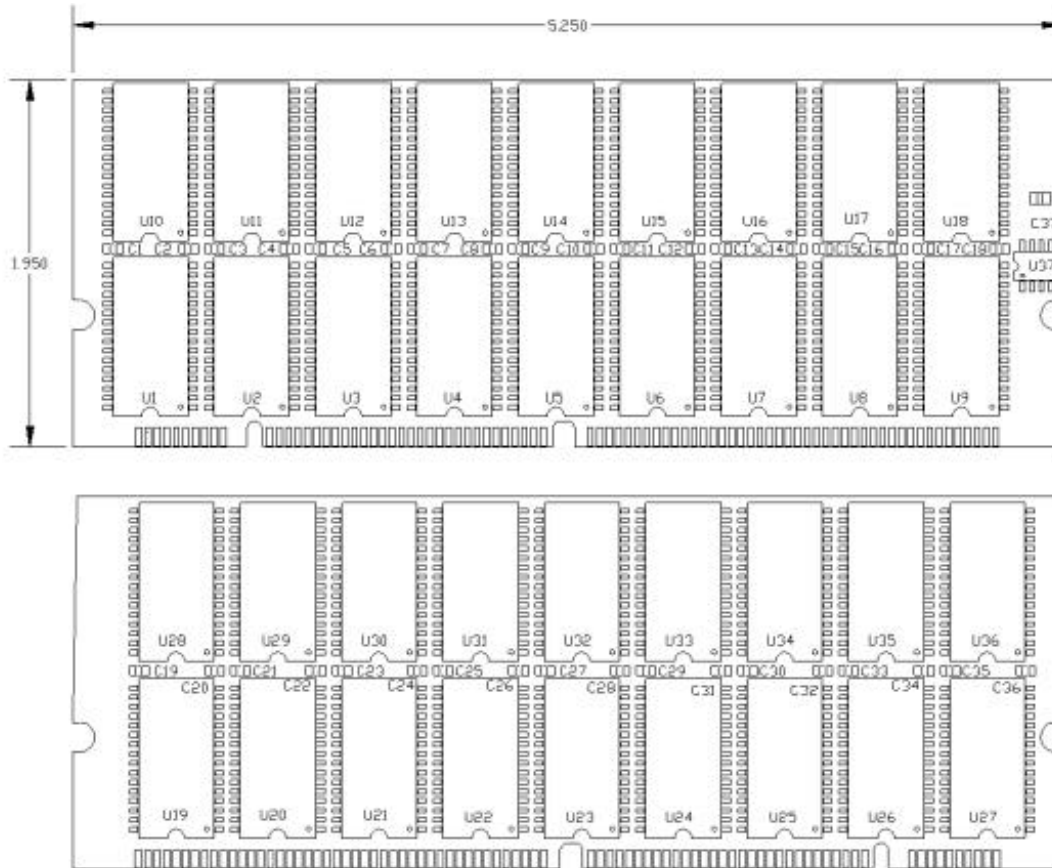
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. VDD = +3.3V; f = 1 MHz.
3. Ice is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100 μ s is required after power-up, followed by eight RAS# REFRESH cycles (RAS*-ONLY or CBR with WE* HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded.
7. AC characteristics assume t_T = 2ns.
8. VIH (MIN) and VIL (MAX) are reference levels for measuring timing of input signals. Transition times are measured between VIH and VIL (or between VIL and VIH).
9. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
10. If CAS# and RAS# = VIH, data output is High-Z.
11. If CAS# = VIL, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and IO_{OP}F and VOL = 0.8V and VOH = 2V.
13. Requires that *-AA and 'CAC are not violated.
14. Requires that tAA and 'RAC are not violated.
15. If CAS* is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ICP.
16. The tRCD (MAX) limit is no longer specified. tRCD (MAX) was specified as a reference point only. If tRCD was greater than the specified tRCD (MAX) limit, then access time was controlled exclusively by tCAC (tRAC [MIN] no longer applied). With or without the tRCD (MAX) limit, tAA and tCAC must always be met.
17. The tRAD (MAX) limit is no longer specified. tRAD (MAX) was specified as a reference point only. If tRAD was greater than the specified tRAD (MAX) limit, then access time was controlled exclusively by tAA (tRAC and *CAC no longer applied). With or without the tRAD (MAX) limit, tAA, tRAC and 'CAC must always be met.
18. Either 'RCH or tRRH must be satisfied for a READ cycle.
19. tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE* = LOW and OE# = HIGH.
21. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
22. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. tWCS, tRWD, tAWD and 'CWD are not restrictive operating parameters. *WCS applies to EARLY WRITE cycles. If WCS > tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. tRWD, tAWD and tCWD define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE# held HIGH and WE# taken LOW after CAS* goes LOW result in a LATE WRITE (OE#-controlled) cycle. 'WCS, tRWD, tCWD and <AWD are not applicable in a LATE WRITE cycle.
24. Column address changed once each cycle.
25. The 3ns minimum parameter guaranteed by design.
26. Measured with the specified current load and IO_{OP}F.
27. 'OFF on an EDO module is determined by the latter of the RAS# and CAS* signals to transition HIGH.
28. The SPD EEPROM WRITE cycle time CWR) is the time from a valid stop condition of a write sequence to the end of the EEPROM Internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit are disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
29. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
30. All other inputs at 0.2V or VDD - 0.2V.
31. VIH overshoot: VIH (MAX) = VDD + 2V for a pulse width < 10ns, and the pulse width cannot be greater than one third of the cycle rate. VIL undershoot: VIL (MIN) = -2V for a pulse width < 10ns, and the pulse width cannot be greater than one third of the cycle rate.



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ENGINEERING DRAWING



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