

**ED1664-16X4-66VNBS4 DRAM DIMM**

16MX64 Unbuffered EDO DIMM based on 16MX4, 4K Refresh, 3.3V DRAMs

**GENERAL DESCRIPTION**

The Advantage ED1664-16X4-66VNBS4 is a JEDEC standard 16MX64 bit Dynamic RAM high density memory module. The Advantage ED1664-16X4-66VNBS4 consists of sixteen CMOS 16MX4 TSOP-II 400mil, EDO Mode DRAM mounted on a 168 pin glass-epoxy substrate. Two 0.1uF (or 0.22uF) decoupling capacitors are mounted on the printed circuit board in parallel for each DRAM. The ED1664-16X4-66VNBS4 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

**FEATURES**

- Row Access Time 60ns
- Column Access Time 17ns
- Random Read/Write Cycle Time 104ns
- Page Mode Cycle Time 25ns
- Refresh Type CAS before RAS (CBR), RAS only, Hidden Refresh
- Refresh Rate 4096 cycles in 64ms

**PIN CONFIGURATIONS (Front/Back)**

1	V <sub>SS</sub>	29	CAS1	57	DQ18	85	V <sub>SS</sub>	113	CAS5	141	DQ50
2	DQ0	30	RAS0	58	DQ19	86	DQ32	114	NC	142	DQ51
3	DQ1	31	OE0	59	V <sub>DD</sub>	87	DQ33	115	NC	143	V <sub>DD</sub>
4	DQ2	32	V <sub>SS</sub>	60	DQ24	88	DQ34	116	V <sub>SS</sub>	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V <sub>DD</sub>	34	A2	62	NC	90	V <sub>DD</sub>	118	A3	146	NC
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	V <sub>SS</sub>	92	DQ37	120	A7	148	NC
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	NC	151	DQ55
12	V <sub>SS</sub>	40	V <sub>DD</sub>	68	V <sub>SS</sub>	96	V <sub>SS</sub>	124	V <sub>DD</sub>	152	V <sub>SS</sub>
13	DQ9	41	V <sub>DD</sub>	69	DQ24	97	DQ41	125	NC	153	DQ56
14	DQ10	42	NC	70	DQ25	98	DQ42	126	NC	154	DQ57
15	DQ11	43	V <sub>SS</sub>	71	DQ26	99	DQ43	127	V <sub>SS</sub>	155	DQ58
16	DQ12	44	OE2	72	DQ27	100	DQ44	128	NC	156	DQ59
17	DQ13	45	RAS2	73	V <sub>DD</sub>	101	DQ45	129	NC	157	V <sub>DD</sub>
18	V <sub>DD</sub>	46	CAS2	74	DQ28	102	V <sub>DD</sub>	130	CAS6	158	DQ60
19	DQ14	47	CAS3	75	DQ29	103	DQ46	131	CAS7	159	DQ61
20	DQ15	48	WE2	76	DQ30	104	DQ47	132	NC	160	DQ62
21	NC	49	V <sub>DD</sub>	77	DQ31	105	NC	133	V <sub>DD</sub>	161	DQ63
22	NC	50	NC	78	V <sub>SS</sub>	106	NC	134	NC	162	V <sub>SS</sub>
23	V <sub>SS</sub>	51	NC	79	NC	107	V <sub>SS</sub>	135	NC	163	NC
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	SA0
26	V <sub>DD</sub>	54	V <sub>SS</sub>	82	SDA	110	V <sub>DD</sub>	138	V <sub>SS</sub>	166	SA1
27	WE0	55	DQ16	83	SCL	111	NC	139	DQ48	167	SA2
28	CAS0	56	DQ17	84	V <sub>DD</sub>	112	CAS4	140	DQ49	168	V <sub>DD</sub>

**PIN NAMES**

A0 ~ A12	Address input
DQ0~DQ63	Data input/output
CB0 ~ 7	Check bit
WE0~WE2	Read/Write Enable
OE0~OE2	Output Enable
RAS~RAS2	Row address strobe
CAS~CAS7	Col. address strobe
VDD	Write enable
VSS	Ground
NC	No connection
SDA	SPD Data
SCL	SPD Clock
SA0 ~ 2	SPD Address

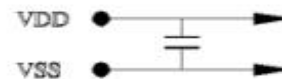
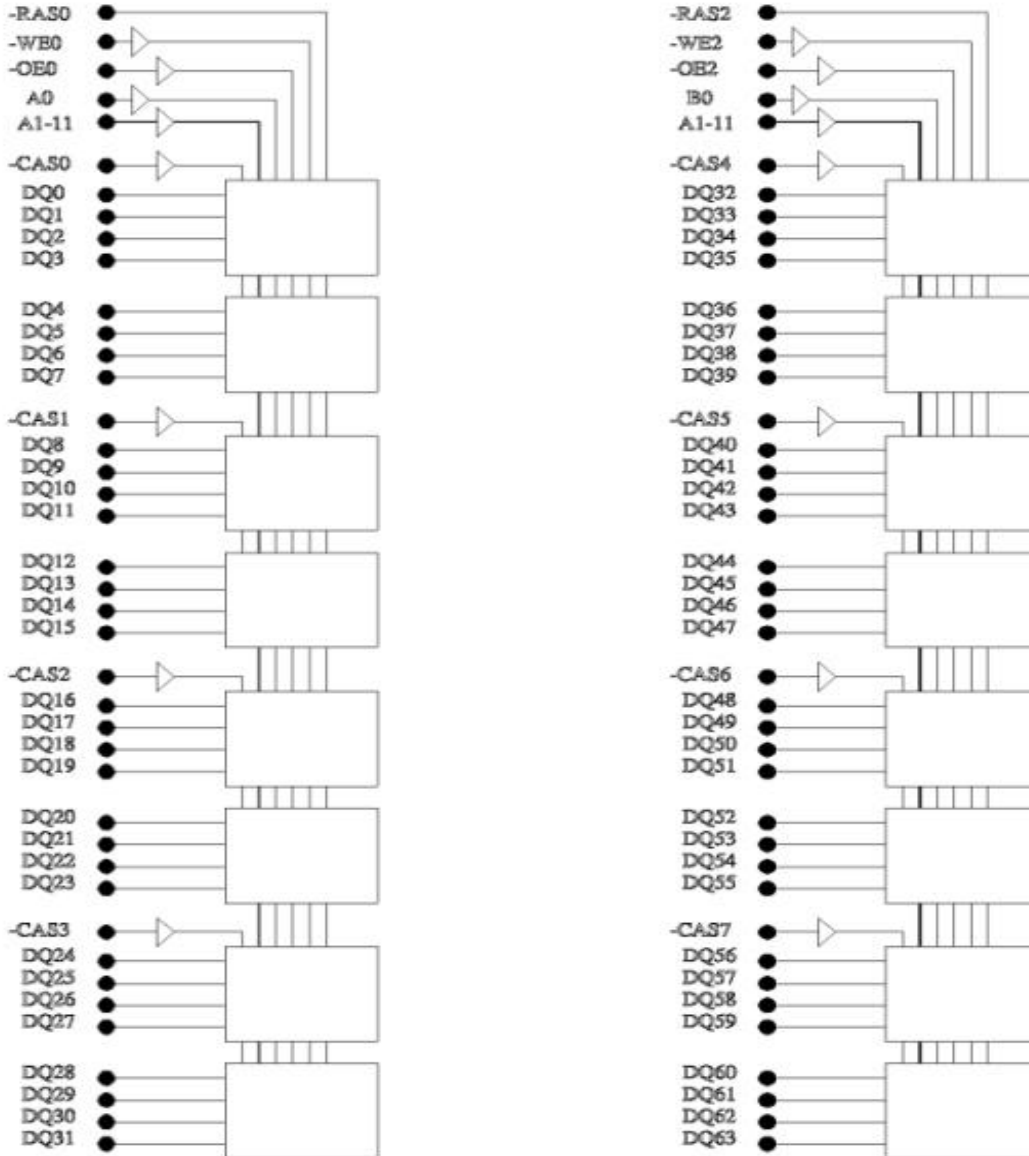
\*These pins are not used on this module  
 \*\*These pins should be NC in the system that does not support SPD



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FUNCTIONAL BLOCK DIAGRAM

168 PIN, X64 DRAM DIMM, 1 BANK WITH X4 DRAMs



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on V <sub>DD</sub> supply relative to Vss	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 4.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Short circuit current	I <sub>OS</sub>	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

Recommended operating conditions (Voltage referenced to V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit
Input leakage (Inputs)	I <sub>IL</sub>		45	uA
Output Leakage Current	I <sub>OL</sub>		5	uA
Output logic high voltage	V <sub>OH</sub>	2.4		V
Output logic low voltage	V <sub>OL</sub>		0.4	V
Operating Current (tRC min)	ICC1		2240	mA
Standby Current (RAS,CAS,W=VIH)	ICC2		16	mA
RAS only refresh Current (RAS cycling)	ICC3		2240	mA
Fast page mode Current (CAS cycling)	ICC4		1760	mA

**CAPACITANCE** (V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 23°C, f = 1MHz, V<sub>REF</sub> = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Input capacitance address bus	CIN1	-	70	pF
Input capacitance RAS	CIN2	-	94	pF
Input capacitance CAS	CIN3	-	52	pF
Input Capacitance WE	CIN4	-	31	pF
Output Capacitance	CDQ	-	17	pF



**AC CHARACTERISTICS**

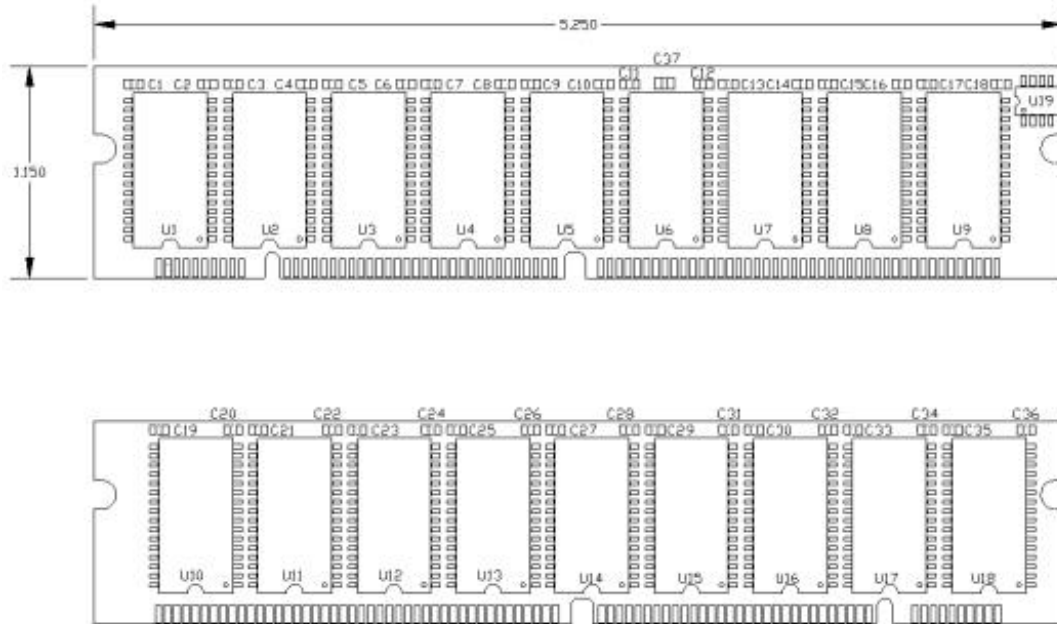
Parameter	Symbol	Min	Max	Unit	Note
Access time from RAS	tRAC		60	ns	
Access time from CAS	tCAS		17	ns	
Random read write cycle time	tRC	104		ns	3,4,7
Fast page mode cycle time	tPC	25		ns	3,4
Access time from column address	tAA		30		3,7
Output buffer turn-off delay	tOFF		15	ns	5
RAS precharge time	tRP	40		ns	
RAS pulse width	tRAS	60	10K	ns	
RAS hold time	tRSH	15		ns	
CAS hold time	tCSH	60		ns	
CAS pulse width	tCAS	10	10K	ns	
RAS to CAS delay time	tRCD	20	43	ns	4
CAS to RAS precharge time	tCRP	5		ns	
Row address set-up time	tASR	0		ns	
Row address hold time	tRAH	10		ns	
Column address set-up time	tASC	0		ns	8
Column address hold time	tCAH	10		ns	8
Write command hold time	tWCH	10		ns	
Command set-up time	tCS	0		ns	6
Data set-up time	tDS	0		ns	6
Data hold time	tDH	10		ns	6
Refresh period	tREF		64	ns	
Read-modify-write cycle	tRWC	104		ns	
CAS precharge time, page cycle	tCP	10		ns	9
RAS pulse width, page cycle	tRASP	60	200K	ns	
OE acces time	tOEA		15	ns	3
OE to data delay	tOED		15	ns	
Output buffer turn off delay	tOEZ	3	15	ns	

1. An initial pause of 200us is required after power-up followed by 8 refresh cycles for proper device operation.
2. VIH(min) and VIL(max) are reference voltage levels for measuring timing of input signals.
3. Measured with a load equivalent of 2 TTL device and 100pf load.
4. Operation within the tRCD(max) limit insures the tRAC(mzx) can be met.
5. Time at which the output achieves the open circuit condition and is not referenced to VOH orVOL.
6. Referenced to CAS leading edge in early write cycles and WE leading edge in RMW cycles.
7. Operation within tRAD(max) limit insures tRAC(max) can be met.
8. TASC, tCAH are referenced to the earlier CAS falling edge.
9. TCP is specified from the last CAS rising edge in the previous cycle ot the first CAS falling edge in the next cycle.



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Engineering Drawing



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