

A836-4X4-66G DRAM SIMM FP

8MX36 DRAM SIMM using 4MX4, 2K Refresh, 5V

GENERAL DESCRIPTION

The Advantage A836-4X4-66G is a 8MX36 Dynamic RAM high-density memory module. The Advantage A836-4X4-66G consists of sixteen CMOS 4MX4 bit DRAMs in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. Two 0.1uF (or 0.22uF) decoupling capacitors are mounted on the printed circuit board in parallel for each DRAM. A836-4X4-66G is a Single In-line Memory Module with edge connections and is intended for mounting into 72-pin edge connector's sockets.

FEATURES

- Part Identification
A836-4X4-66G
- Fast Page Mode Operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V+/- 10% power supply
- JEDEC standard PDPin & pinout
- PCB: **Height (1.175mil)** double sided component

PIN CONFIGURATIONS (Front/Back)

1	V _{ss}	29	A11	57	DQ13
2	DQ0	30	V _{cc}	58	DQ31
3	DQ18	31	A8	59	V _{cc}
4	DQ1	32	A9	60	DQ32
5	DQ19	33	Res(RAS1)	61	DQ14
6	DQ2	34	RAS0	62	DQ33
7	DQ20	35	DQ26	63	DQ15
8	DQ3	36	DQ8	64	DQ34
9	DQ21	37	DQ17	65	DQ16
10	V _{cc}	38	DQ35	66	NC
11	NC	39	V _{ss}	67	PD1
12	A0	40	CAS0	68	PD2
13	A1	41	CAS2	69	PD3
14	A2	42	CAS3	70	PD4
15	A3	43	CAS1	71	NC
16	A4	44	RAS0	72	V _{ss}
17	A5	45	Res(RAS1)		
18	A6	46	NC		
19	A10	47	W		
20	DQ4	48	NC		
21	DQ22	49	DQ9		
22	DQ5	50	DQ27		
23	DQ23	51	DQ10		
24	DQ6	52	DQ28		
25	DQ24	53	DQ11		
26	DQ7	54	DQ29		
27	DQ25	55	DQ12		
28	A7	56	DQ30		

PIN NAMES

A0~A10	Address Inputs (2K)
DQ0~DQ35	Data input/output
W	Read/Write Enable
<u>RAS0, RAS1</u>	Row Address Strobe
<u>CAS0~CAS3</u>	Col. address strobe
<u>PD1~PD4</u>	Presence Detect
V _{cc}	Power (+5V)
V _{ss}	Ground
NC	No Connection

*These pins are not used on this module
 **These pins should be NC in the system that does not support SPD



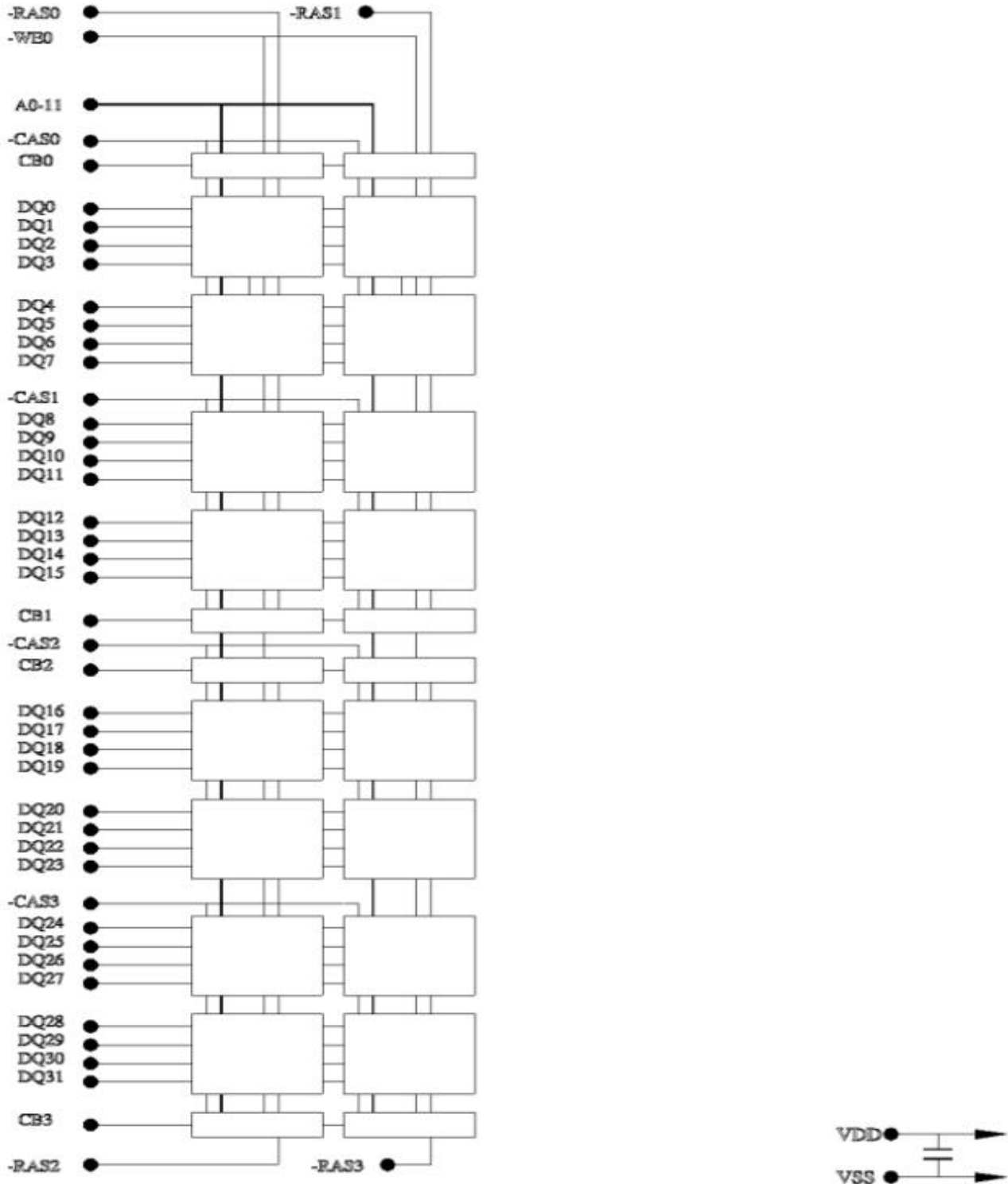
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address: RA0 ~ RA11, Column address: CA0 ~ CA9
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
W	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, WE active.
DQ0 ~ DQ31	Input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.



FUNCTIONAL BLOCK DIAGRAM

72 PIN X36 DRAM SIMM, 2 BANKS WITH X4 AND X1 DRAMS



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 7.0	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 7.0	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _d	18	W
Short circuit current	I _{OS}	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	2.0	0	0	V
Input high voltage	V _{IH}	2.4	-	V _{CC} +1*1	V
Input low voltage	V _{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}

*2 : -2.0V/20ns, Pulse width is measured at V_{SS}

CAPACITANCE (V_{CC} = 5V, T_A = 25°C, f = 1MHz,

Pin	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	C _{N1}	-	110	pF
Input capacitance[W]	C _{N2}	-	130	pF
Input capacitance[RAS0]	C _{N3}	-	80	pF
Input capacitance[CAS0-CAS3]	C _{N4}	-	40	pF
Input/Output capacitance[DQ0-31]	C _{DQ1}	-	25	pF



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DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Speed	A836-4X4-66G		Unit
			Min	Max	
Operating current	Icc1	-C50 -C60	- -	1008 918	mA
Standby Current	Icc2	Don't care	-	36	mA
RAS Only Refresh Current	Icc3	-C50 -C60	- -	1008 918	mA
EDO Mode Current	Icc4	-C50 -C60	- -	828 738	mA
Standby Current	Icc5	Don't care	-	18	mA
CAS-Before-RAS Refresh Current	Icc6	-C50 -C60	- -	1008 918	mA
Input Leakage Current	IIL	Don't care	-90	90	uA
Output Leakage Current	IOL	Don't care	-10	10	uA
Output High Voltage Level	V IH	Don't care	2.4	-	V
Output Low Voltage Level	V OL	Don't care	-	0.4	V

- Icc1 : Operating Current * ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address cycling @trc=min)
- Icc2 : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\text{W}=\text{V}_{\text{IH}}$)
- Icc3 : RAS Only Refresh Current * ($\overline{\text{CAS}}=\text{V}_{\text{IH}}$, $\overline{\text{RAS}}$ cycling @trc=min)
- Icc4 : EDO Mode Current * ($\overline{\text{RAS}}=\text{V}_{\text{IL}}$, $\overline{\text{CAS}}$ Address cycling : tHPC=min)
- Icc5 : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\text{W}=\text{V}_{\text{CC}}-0.2\text{V}$)
- Icc6 : CAS-Before-RAS Refresh Current * ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling @trc=min)
- I(L) : Input Leakage Current (Any input $0 < \text{V}_{\text{IN}} < \text{V}_{\text{CC}} + 0.5\text{V}$, all other pins not under test=0 V)
- I(O(L) : Output Leakage Current (Data Out is disabled, $0\text{V} < \text{V}_{\text{OUT}} < \text{V}_{\text{CC}}$)
- V OH : Output High Voltage Level (I OH = -5mA)
- V OL : Output Low Voltage Level (I OL = 4.2mA)

***NOTE:** Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while RAS=VIL. In Icc4, address can be changed maximum once within one EDO mode cycle, tHPC.



AC CHARACTERISTICS

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	1
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	
Access time from $\overline{\text{CAS}}$	tCAC		13		15	ns	1
Access time from column address	tAA		25		30	ns	1
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		us	
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	0	13	0	15	ns	1
Transition time(rise and fall)	tT	3	50	3	50	ns	
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	ns	
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	1
Row address set-up time	tASR	0		0		ns	1
Row address hold time	tRAH	10		10		ns	4
Column address set-up time	tASC	0		0		ns	5
Column address hold time	tCAH	10		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	4
Read command set-up time	tRCS	0		0		ns	5
Read command hold time referenced to $\overline{\text{CAS}}$	tRAL	0		0		ns	3
Read command hold time referenced to $\overline{\text{RAS}}$	tRCH	0		0		ns	3
Write command hold time	tRRH	10		10		ns	3
Write command pulse width	tWCH	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tWP	13		15		ns	2
Write command to $\overline{\text{CAS}}$ lead time	tRWL	13		15		ns	
Data-in set-up time	tCWL	0		0		ns	
Data-in hold time	tDS	10		15		ns	
Refresh period (4K Ref)	tDH		0		0	ms	
Refresh period (2K Ref)	tREF		32		32	ms	
Write command set-up time	tREF	0		0		ns	
$\overline{\text{CAS}}$ setup time($\overline{\text{CAS}}$ -before $\overline{\text{RAS}}$ refresh)	tCSR	5		5		ns	
$\overline{\text{CAS}}$ hold time($\overline{\text{CAS}}$ -before $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		ns	
$\overline{\text{CAS}}$ precharge time (C-B-R counter test)	tCPT	2		20		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35	ns	
Hyper page mode cycle time	tHPC	35		40		ns	
$\overline{\text{CAS}}$ precharge time(Hyper page cycle)	tCP	10		10		ns	
$\overline{\text{RAS}}$ pulse width(Hyper page cycle)	tRASP	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		ns	
W to $\overline{\text{RAS}}$ precharge time(C-B-R refresh)	tWRP	10		10		ns	
W to $\overline{\text{RAS}}$ hold time (C-B-R refresh)	tWRH	10		10		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	3	13	3		ns	
Output buffer turn off delay from W	tWEZ	3	13	3		ns	
W to data delay	tWED	15		15		ns	
W pulse width (Hyper Page Cycle)	tWPE	5		5		ns	

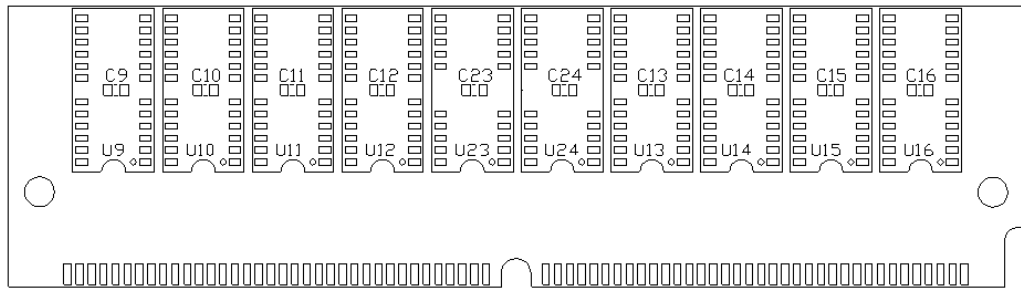
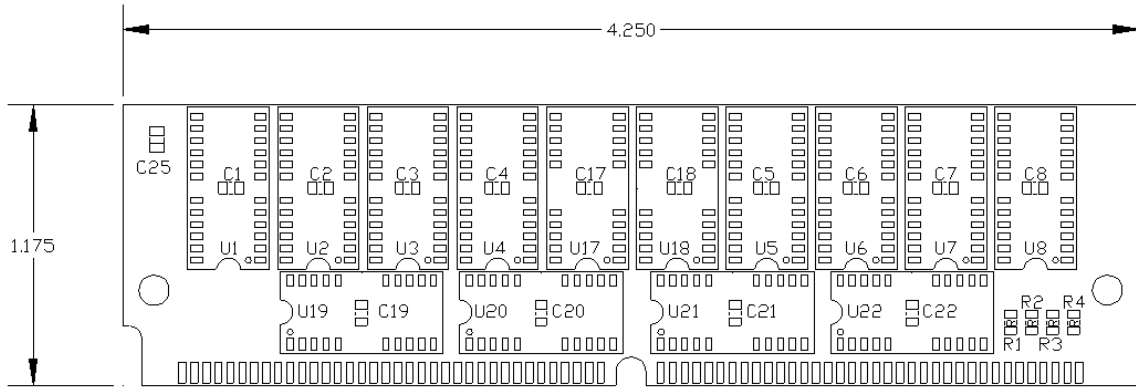


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Notes

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before Proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring Timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} > t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameter are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures That $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. $t_{\text{CEZ}}(\text{max})$, $t_{\text{REZ}}(\text{max})$, $t_{\text{WEZ}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
12. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
13. $t_{\text{ASC}} > t_{\text{CP min}}$





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