

A132-1X16-67T DRAM SIMM FPM

1MX32 DRAM SIMM using 1MX16, 1K Refresh, 5V

GENERAL DESCRIPTION

The Advantage A132-1X16-67T is a 1MX16 Dynamic RAM high-density memory module. The Advantage A132-1X16-67T consists of two CMOS 1MX16 bit DRAMs in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. Two 0.1uF (or 0.22uF) decoupling capacitors are mounted on the printed circuit board in parallel for each DRAM. The A132-1X16-67T is a Single In-line Memory Module with edge connections and is intended for mounting into 72-pin edge connectors sockets.

FEATURES

- Part Identification
A132-1X16-67T
- Fast Page Mode Operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V+/- 10% power supply
- JEDEC standard PDPin & pinout
- PCB: **Height(1,000mil)**, single sided component

PIN CONFIGURATIONS (Front/Back)

1	V _{ss}	29	A11	57	DQ13
2	DQ1	30	V _{cc}	58	DQ29
3	DQ17	31	A8	59	V _{cc}
4	DQ2	32	A9	60	DQ30
5	DQ18	33	RAS3	61	DQ14
6	DQ3	34	RAS2	62	DQ31
7	DQ19	35	NC	63	DQ15
8	DQ4	36	NC	64	DQ32
9	DQ20	37	NC	65	DQ16
10	V _{cc}	38	NC	66	NC
11	NC	39	V _{ss}	67	PD1
12	A0	40	CAS0	68	PD2
13	A1	41	CAS2	69	PD3
14	A2	42	CAS3	70	PD4
15	A3	43	CAS1	71	NC
16	A4	44	RAS0	72	V _{ss}
17	A5	45	Res(RAS1)		
18	A6	46	NC		
19	A10	47	WE		
20	DQ5	48	NC		
21	DQ21	49	DQ9		
22	DQ6	50	DQ25		
23	DQ22	51	DQ10		
24	DQ7	52	DQ26		
25	DQ23	53	DQ11		
26	DQ8	54	DQ27		
27	DQ24	55	DQ12		
28	A7	56	DQ28		

PIN NAMES

A0 ~ A11	Address inputs(4K)
A0~A10	Address Inputs(2K)
DQ0~DQ31	Data input/output
\overline{W}	Read/Write Enable
$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0-CAS3}$	Col. address strobe
PD1~PD4	Presence Detect
V _{cc}	Power(+5V)
V _{ss}	Ground
NC	No Connection

*These pins are not used on this module
 **These pins should be NC in the system that does not support SPD



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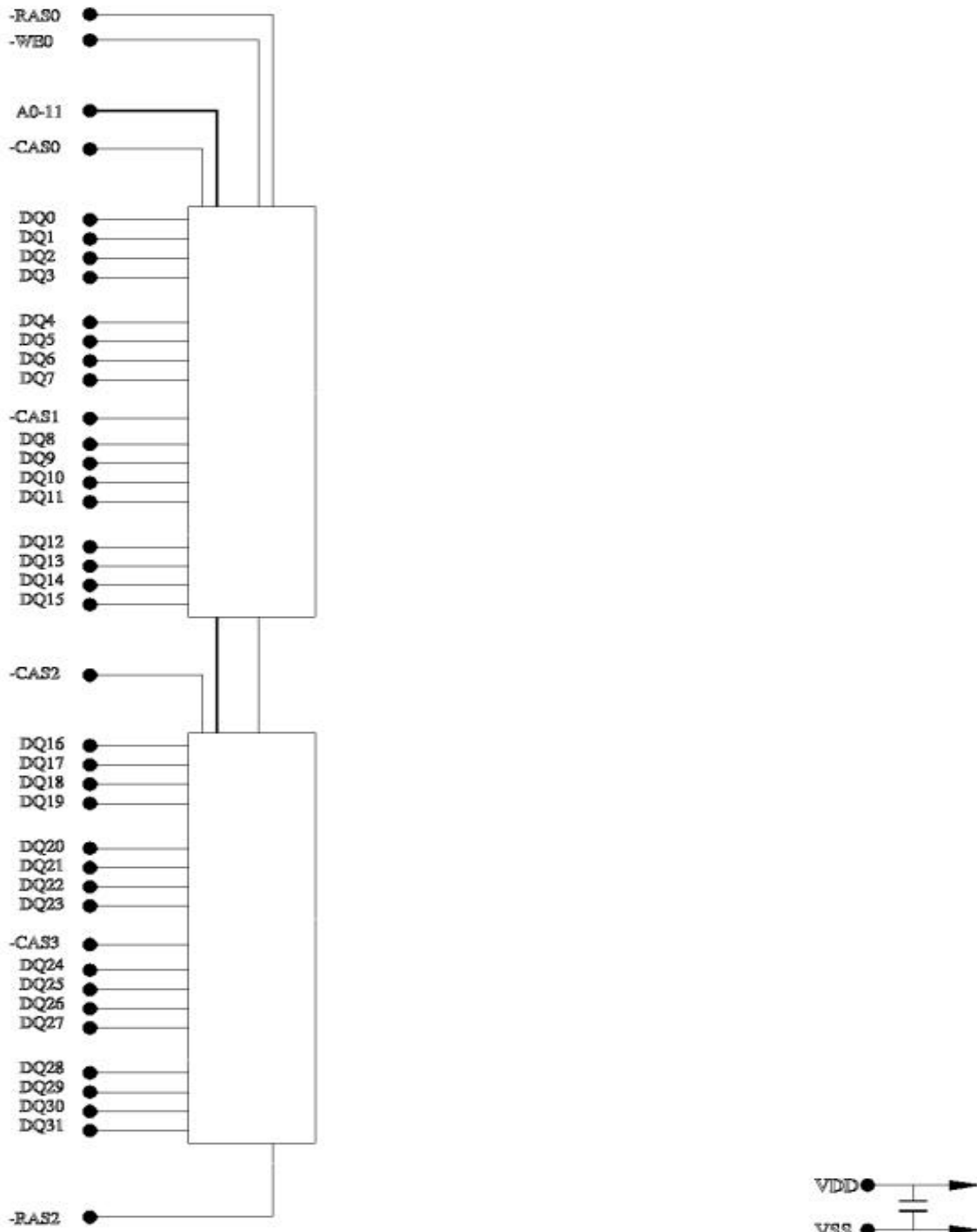
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
$\overline{\text{RAS}}$	Row address strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column address strobe	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
W	Write enable	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, WE active.
DQ0 ~ DQ31	input/output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.



FUNCTIONAL BLOCK DIAGRAM

72 PIN X32 DRAM SIMM, 1 BANK WITH X16 DRAMS



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 7.0	V
Voltage on V _{DD} supply relative to Vss	V _{DD} , V _{DDQ}	-1.0 ~ 7.0	V
Storage temperature	T _{STG}	-55 ~ +125	°C
Power dissipation	P _d	8	W
Short circuit current	I _{OS}	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to recommended condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	2.0	0	0	V
Input high voltage	V _{IH}	2.4	-	V _{CC} +1*1	V
Input low voltage	V _{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}

*2 : -2.0V/20ns, Pulse width is measured at V_{SS}

CAPACITANCE (V_{CC} = 5V, T_A = 25°C, f = 1MHz)

Pin	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	C _{N1}	-	48	pF
Input capacitance[W]	C _{N2}	-	64	pF
Input capacitance[RAS0]	C _{N3}	-	32	pF
Input capacitance[CAS0-CAS3]	C _{N4}	-	16	pF
Input/Output capacitance[DQ0-31]	C _{DQ1}	-	10	pF



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DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Speed	A132-1X16-67T		Unit
			Min	Max	
Operating current	Icc1	-50 -60	- -	- 880	mA
Standby Current	Icc2	Don't care	-	16	mA
RAS Only Refresh Current	Icc3	-50 -60	- -	- 880	mA
EDO Mode Current	Icc4	-50 -60	- -	- -	mA
Standby Current	Icc5	Don't care	-	8	mA
CAS-Before-RAS Refresh Current	Icc6	-50 -60	- -	- 880	mA
Input Leakage Current	IIL	Don't care	-	32	uA
Output Leakage Current	IOL	Don't care	-	5	uA
Output High Voltage Level	V _{IH}	Don't care	-2.4	-	V
Output Low Voltage Level	V _{OL}	Don't care	-	0.4	V

- Icc1 : Operating Current * ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address cycling @trc=min)
- Icc2 : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{IH}}$)
- Icc3 : RAS Only Refresh Current * ($\overline{\text{CAS}}=\text{V}_{\text{IH}}$, $\overline{\text{RAS}}$ cycling @trc=min)
- Icc4 : EDO Mode Current * ($\overline{\text{RAS}}=\text{V}_{\text{IL}}$, $\overline{\text{CAS}}$ Address cycling : tHPC=min)
- Icc5 : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{CC}}-0.2\text{V}$)
- Icc6 : CAS-Before-RAS Refresh Current * ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling @trc=min)
- I_(L) : Input Leakage Current (Any input $0 < \text{V}_{\text{IN}} < \text{V}_{\text{CC}} + 0.5\text{V}$, all other pins not under test=0 V)
- I_{o(L)} : Output Leakage Current (Data Out is disabled, $0\text{V} < \text{V}_{\text{OUT}} < \text{V}_{\text{CC}}$)
- V_{OH} : Output High Voltage Level (I_{OH} = -5mA)
- V_{OL} : Output Low Voltage Level (I_{oL} = 4.2mA)

***NOTE:** Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while RAS=V_{IL}. In Icc4, address can be changed maximum once within one EDO mode cycle, tHPC.



AC CHARACTERISTICS

Parameter	Symbol	-60		Unit	Note
		Min	Max		
Random read or write cycle time	trc	110		ns	1
Access time from $\overline{\text{RAS}}$	trAC		60	ns	
Access time from $\overline{\text{CAS}}$	tcAC		15	ns	1
Access time from column address	tAA		30	ns	1
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3	15	ns	
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	50	ns	1
Transition time(rise and fall)	ttT	2		ns	
$\overline{\text{RAS}}$ precharge time	trP	40	10K	ns	
$\overline{\text{RAS}}$ pulse width	trAS	60		ns	
$\overline{\text{RAS}}$ hold time	trSH	15		ns	
$\overline{\text{CAS}}$ hold time	tcSH	45	10K	ns	
$\overline{\text{CAS}}$ pulse width	tcAS	10	45	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	trCD	20	30	ns	
$\overline{\text{RAS}}$ to column address delay time	trAD	15		ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tcRP	5		ns	1
Row address set-up time	tASR	0		ns	1
Row address hold time	trAH	10		ns	4
Column address set-up time	tASC	0		ns	5
Column address hold time	tcAH	30		ns	4
Read command set-up time	trCS	0		ns	5
Read command hold time referenced to $\overline{\text{CAS}}$	trAL	0		ns	3
Read command hold time referenced to $\overline{\text{RAS}}$	trCH	0		ns	3
Write command hold time	trRH	10		ns	3
Write command pulse width	twCH	10		ns	
Write command to $\overline{\text{RAS}}$ lead time	twP	15		ns	2
Write command to $\overline{\text{CAS}}$ lead time	trWL	10		ns	
Data-in set-up time	tcWL	0		ns	
Data-in hold time	tdS	10		ns	
Refresh period (4K Ref)	tdH		64	ms	
Refresh period (2K Ref)	trEF		32	ms	
Write command set-up time	trEF	0		ns	
$\overline{\text{CAS}}$ setup time($\overline{\text{CAS}}$ -before $\overline{\text{RAS}}$ refresh)	tcSR	5		ns	
$\overline{\text{CAS}}$ hold time($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		ns	
$\overline{\text{CAS}}$ precharge time (C-B-R counter test)	tcPT	20		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		35	ns	
Hyper page mode cycle time	thPC	30		ns	
$\overline{\text{CAS}}$ precharge time(Hyper page cycle)	tcP	10		ns	
$\overline{\text{RAS}}$ pulse width(Hyper page cycle)	trASP	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	35		ns	
W to $\overline{\text{RAS}}$ precharge time(C-B-R refresh)	twRP	10		ns	
W to $\overline{\text{RAS}}$ hold time (C-B-R refresh)	twRH	10		ns	
Output data hold time	tdOH	5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	trEZ	3		ns	
Output buffer turn off delay from W	twEZ	3		ns	
W to data delay	twED	15		ns	
W pulse width (Hyper Page Cycle)	twPE	5		ns	

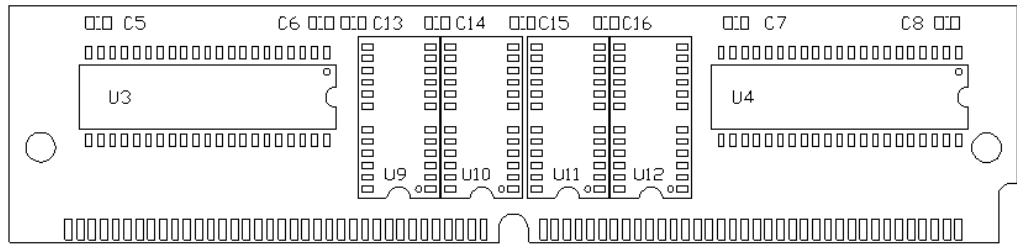
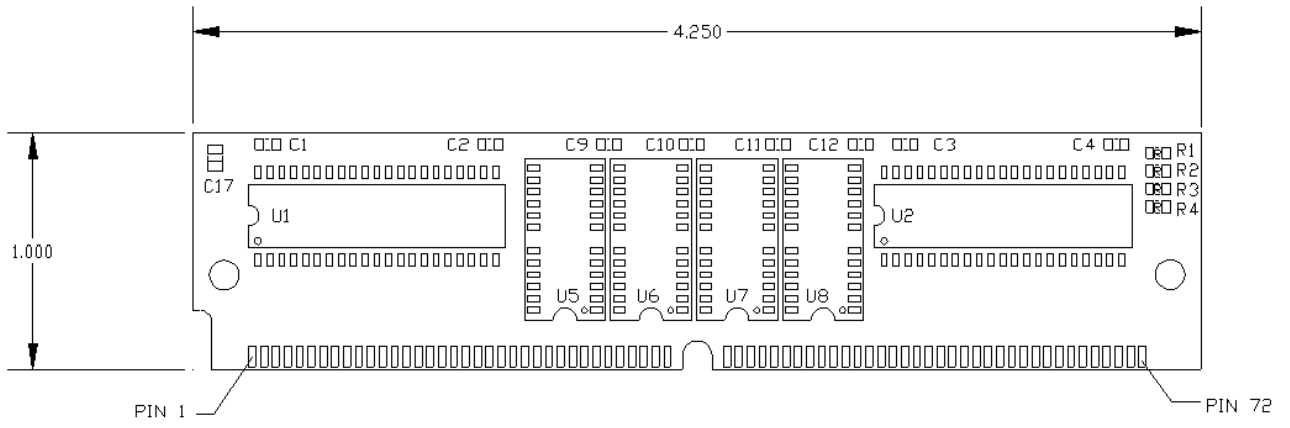


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Notes

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before Proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring Timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} > t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameter are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures That $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. $t_{\text{CEZ}}(\text{max})$, $t_{\text{REZ}}(\text{max})$, $t_{\text{WEZ}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
12. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
13. $t_{\text{ASC}} > t_{\text{CP min}}$





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